FINAL EXAMINATION SOLUTIONS

Electronics I for ME
Course Number ECE 09-311 2
CRN 20462

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Problem 1 (25%)

In the simple resistor-capacitor (RC) circuit shown in Figure 1 below, the input voltage is a sine wave,

$$v_{IN}(t) = V_P \cdot \cos(\omega \cdot t).$$

Find the steady-state sine wave output voltage $v_{OUT}(t)$ as a function of the resistance R, the capacitor C, the peak input voltage V_P, the angular frequency ω, and time t. Use the concept of complex impedance. To do this,

- Show the complex form $vz_{IN}(t)$ for the input voltage such that $v_{IN}(t)$ is the real part of $vz_{IN}(t)$ and $vz_{IN}(t)$ has constant complex amplitude with time.
- Derive and show the voltage across the capacitor C in either real or complex format.
- Provide the complex voltage transfer function $G(\omega)$ that, when multiplied by $vz_{IN}(t)$, yields the complex form of the output voltage across the resistor R.

Your solution should be of the form

$$\begin{aligned} v_{OUT}(t) &= \operatorname{Re}\{vz_{OUT}(t)\} \\ &= \operatorname{Re}\{G(\omega) \cdot vz_{IN}(t)\} \end{aligned}$$

where $G(\omega)$ is the ratio of simple complex polynomials in ω.

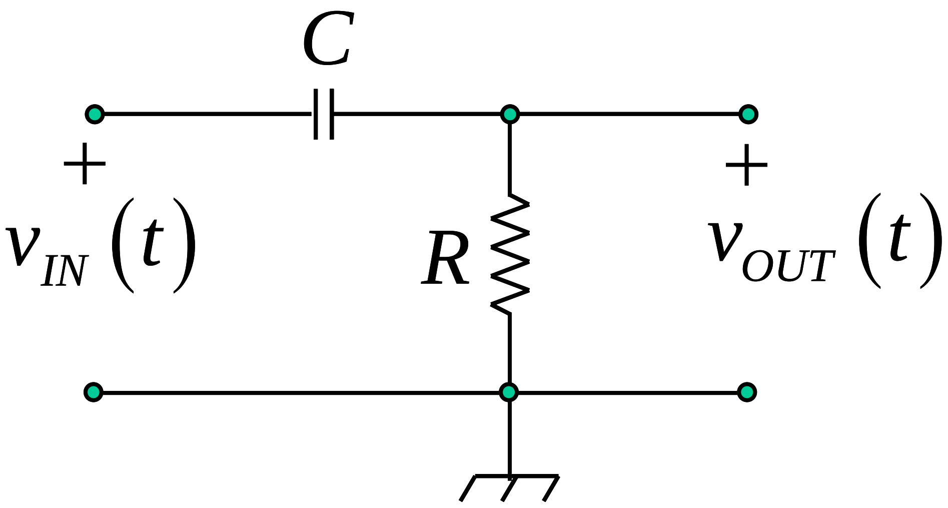

Figure 1. Simple RC Circuit for Problem 1.

Solution

We specify that the complex magnitude of the input waveform, in complex notation, be constant. This was given in Chapter 1 and the first lectures, and is available on the course web site as notes on the first lecture. Here we will derive it from first principles.

The complex form of the input waveform is

(1.1) $$vz(t) = V_P \cdot \cos(\omega \cdot t) + j \cdot vzy(t)$$

where the imaginary part $vzy(t)$ is to be found. The square of the complex magnitude of $vz(t)$ is

(1.2) $$|vz(t)|^2 = V_P^2 \cdot (\cos(\omega \cdot t))^2 + (vzy(t))^2$$

and we have specified that the complex magnitude be constant in time. Thus

(1.3) $$\frac{d}{dt}|vz(t)|^2 = 0 = -2 \cdot V_P^2 \cdot \cos(\omega \cdot t) \cdot \sin(\omega \cdot t) + \frac{d}{dt}(vzy(t))^2$$

and we have

(1.4) $$\frac{d}{dt}(vzy(t))^2 = V_P^2 \cdot \sin(2 \cdot \omega \cdot t)$$

so that

(1.5) $$(vzy(t))^2 = V_P^2 \cdot \frac{1 - \cos(2 \cdot \omega \cdot t)}{2} + Const = (V_p \cdot \sin(\omega \cdot t))^2 + Const\,.$$

If we ask that the mean value of $vzy(t)$ over time to be zero, the constant of integration is zero, and we select the positive sign for the square root and we have the complex form of the input as

(1.6) $$vz_{IN}(t) = V_P \cdot \exp(j \cdot \omega \cdot t)\,.$$

We are instructed in the problem statement to use the concept of complex impedance. With that context, we need the impedance of the capacitor,

(1.7) $$Z_C = \frac{1}{j \cdot \omega \cdot C}\,.$$

The circuit in Figure 1 is a simple voltage divider. Its output is

(1.8) $$vz_{OUT}(t) = \frac{R}{R + Z_C} \cdot vz_{IN}(t) = \frac{j \cdot \omega \cdot R \cdot C}{1 + j \cdot \omega \cdot R \cdot C} \cdot vz_{IN}(t)\,.$$

The complex transfer function is

(1.9) $$G(\omega) = \frac{vz_{OUT}(t)}{vz_{IN}(t)} = \frac{j \cdot \omega \cdot R \cdot C}{1 + j \cdot \omega \cdot R \cdot C}\,.$$

Problem 2 (25%)

Figure 1 below is a simple model of the IRFZ24N MOSFET from IRC that offers a reasonable approximation of the v-i curves in the IRC data sheet for an ambient temperature of 25 C. The transition voltage V_{TR} for this model is 2.75 Volts. Consider the electromagnet a simple resistive load. Assume that the PIC microcontroller provides 5.0 Volts of drive for the MOSFET gate. Draw the load line for electromagnet resistances of 1.25 Ohms on Figure 3. Give the steady-state DC current through the electromagnet. Compare that current with the current that would be produced by 5 Volts across the electromagnet.

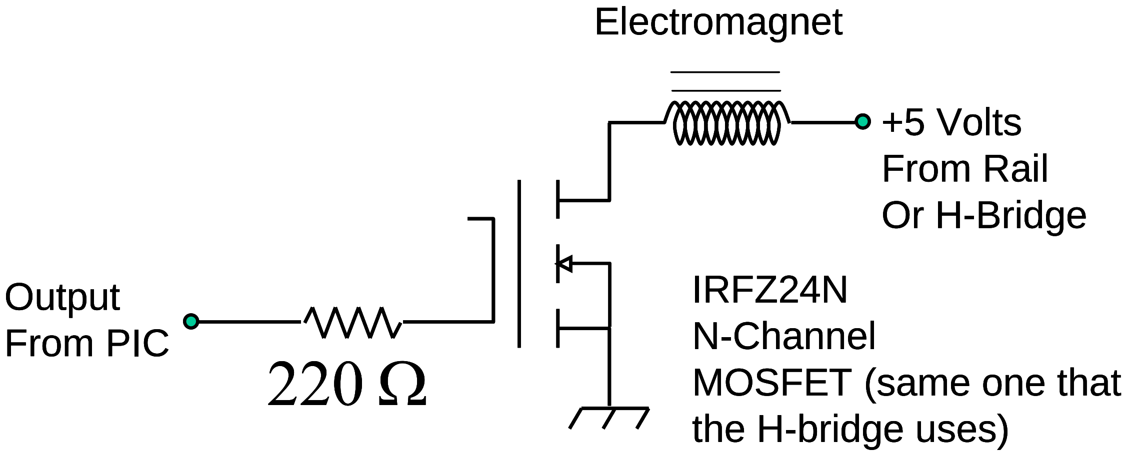

Figure 2. Microcontroller Operated Electromagnet Driver from 5 Volts Using the IRFZ24N MOSFET

Solution

The load line intersects the 5 Volt drive v-i curve at 3.45 Amperes. A direct connection of 5 Volts across the electromagnet provides 4 Amperes. Thus the MOSFET switch will produce about 86% the drive current as a direct connection.

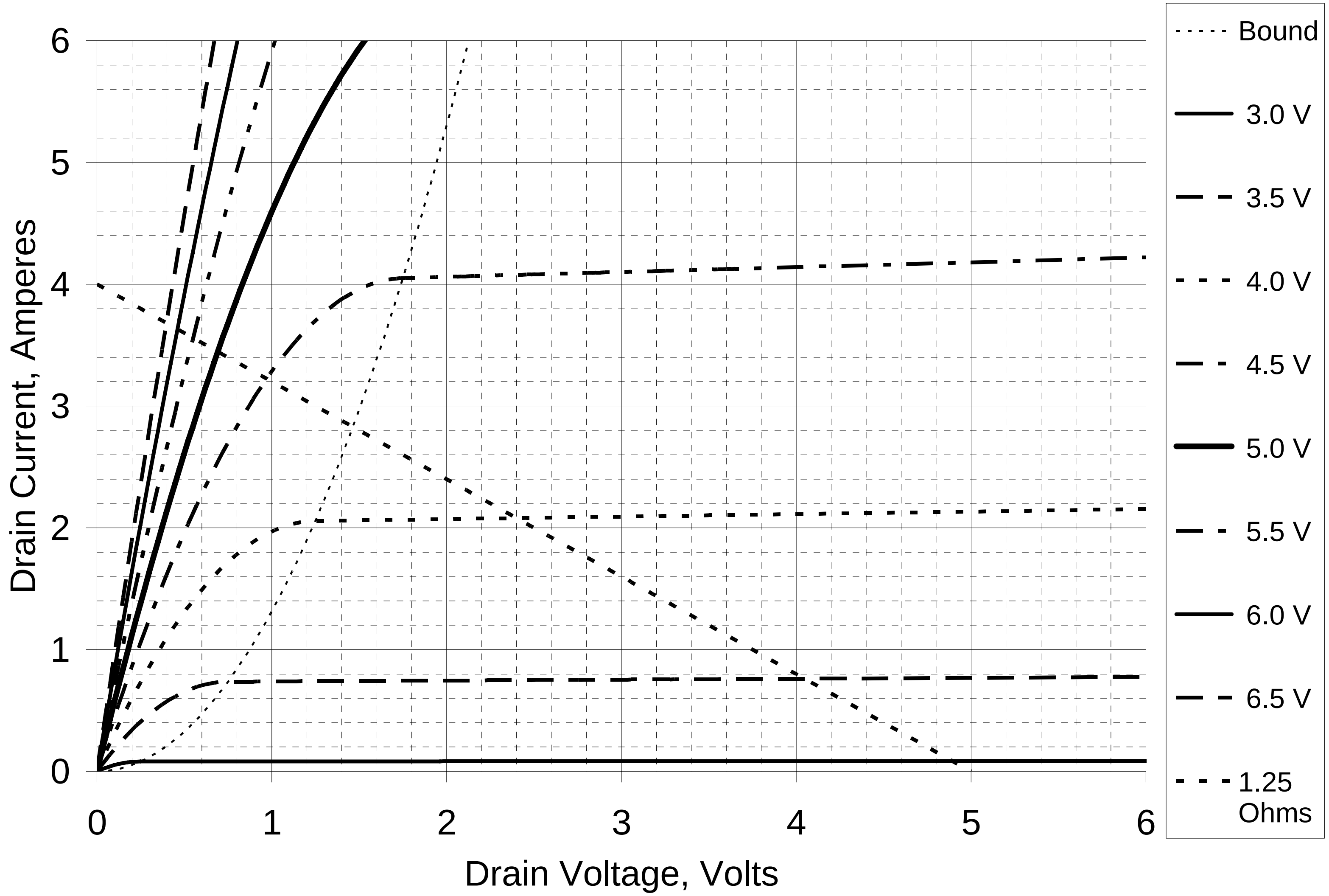

Figure 3. V-i Curves from a Model of the IRFZ24N MOSFET.

Problem 3 (25%)

Refer to Figure 4 for the circuit for this problem and Figure 5 for the v-i curves for the MOSFET in the circuit. The threshold voltage V_{TR} is 2.0 Volts for this MOSFET. Ignore the effects of the gate resistor R_G for this problem. For a supply voltage V_{DD} of 25 Volts and a load resistance R_D of 0.5 Ohms, plot the output voltage e_{OUT} as the Y axis versus the input voltage e_{IN} as the X axis. To do this,

- Draw a load line on Figure 5.
- For values of e_{IN} from 2.0 Volts to 10.0 Volts in increments of 1.0 Volt, find the output voltage e_{OUT} from your load line and its intersections with the appropriate v-i curves in Figure 5, and make a table of e_{OUT} versus e_{IN}.
- Draw your plot using the table.

On the plot, mark the point where the transistor is cut off, where the transistor transits from the constant current region to the triode region, and the saturation point.

Special essay response: In a few sentences, tell how the output impedance of 0.5 ohms for this circuit might be interfaced with a 4 Ohm speaker. Comment on the linearity of this amplifier. Estimate the maximum continuous RMS power of this amplifier with a sine wave output.

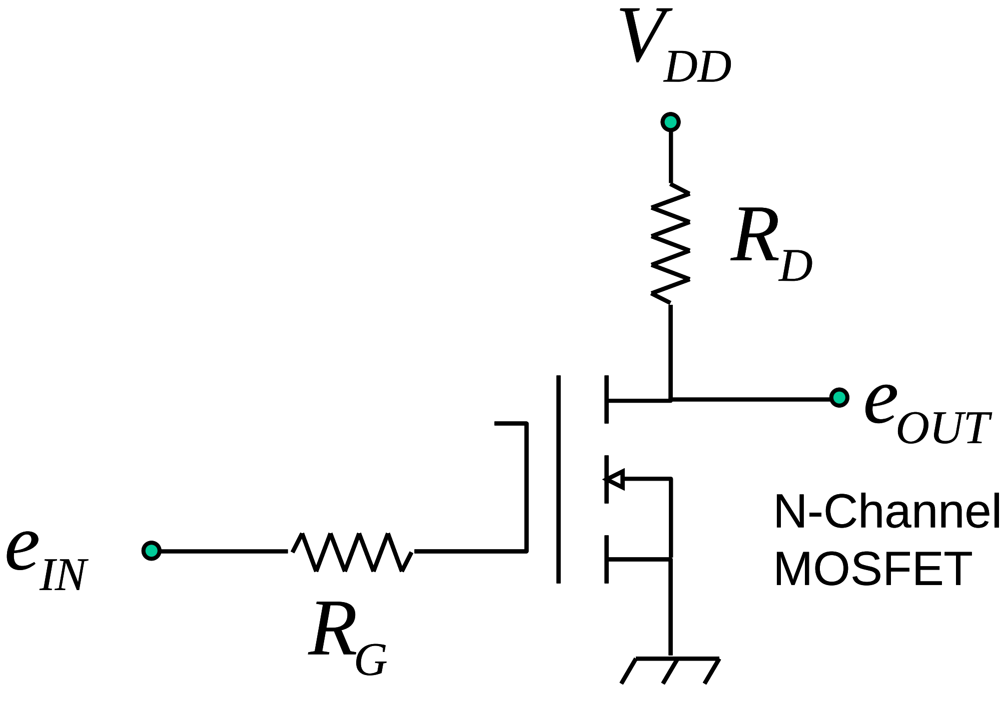

Figure 4. Circuit for Problem 4.

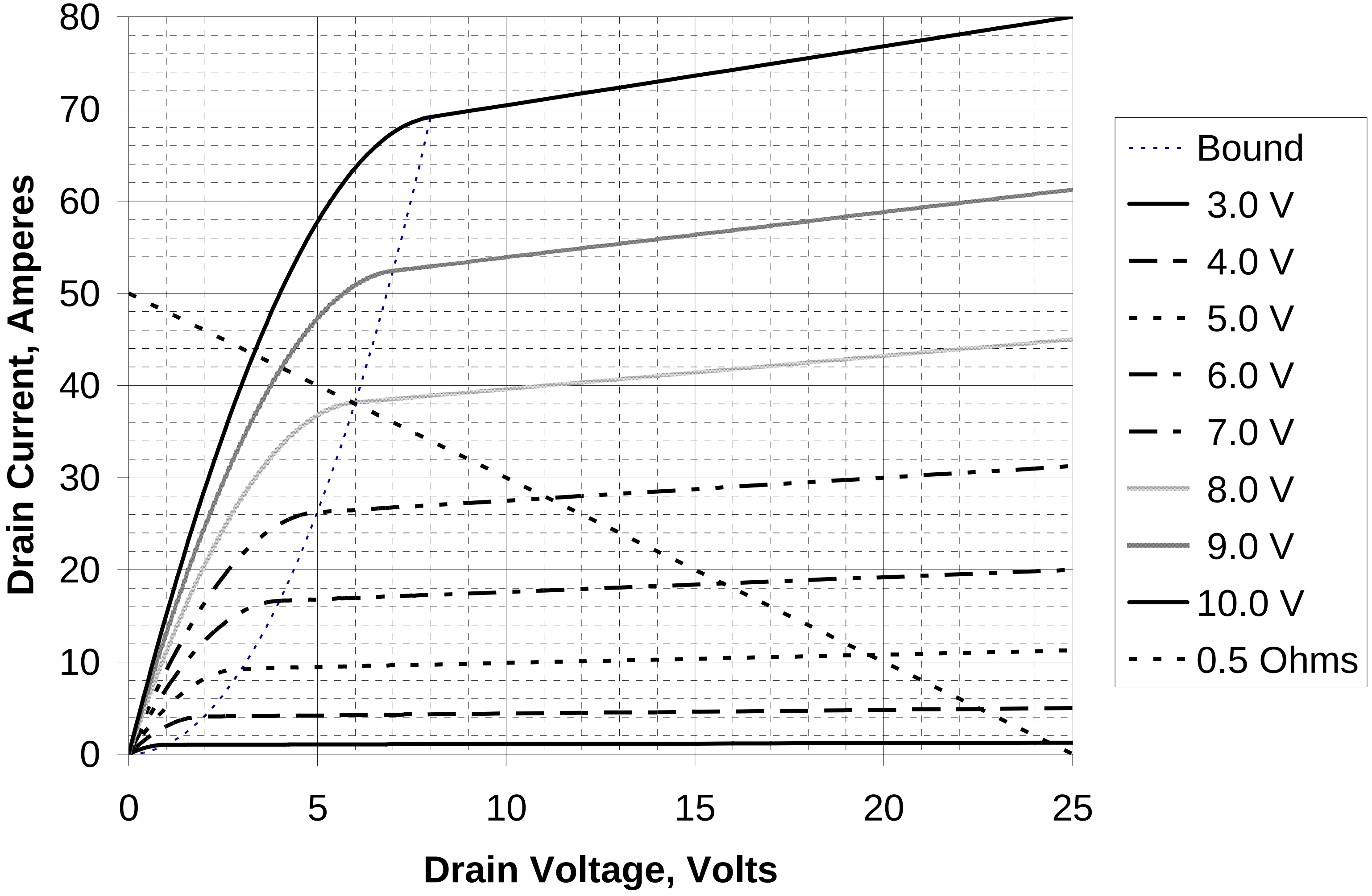

Figure 5. V-i Curves for a MOSFET.

Solution

The load line for a collector resistance of 0.5 Ohms is drawn on Figure 5. The intersections of the load line with the v-i curves for gate voltages from 2.0 Volts to 10 volts in 1 Volt increments is shown below as Table 1 below. Note that 2.0 Volts is V_{TR} as given in the problem statement so that the drain current is zero for this value of v_G.

Table 1. Drain Voltage vs. Gate Voltage from Load Line and v-i Curves.

e_{IN}, Volts	e_{OUT} from load line, Volts
2	25
3	24.4
4	22.6
5	19.6
6	15.7
7	11.1
8	5.9
9	4.0
10	3.3

From Table 1 we construct the plot shown below as .

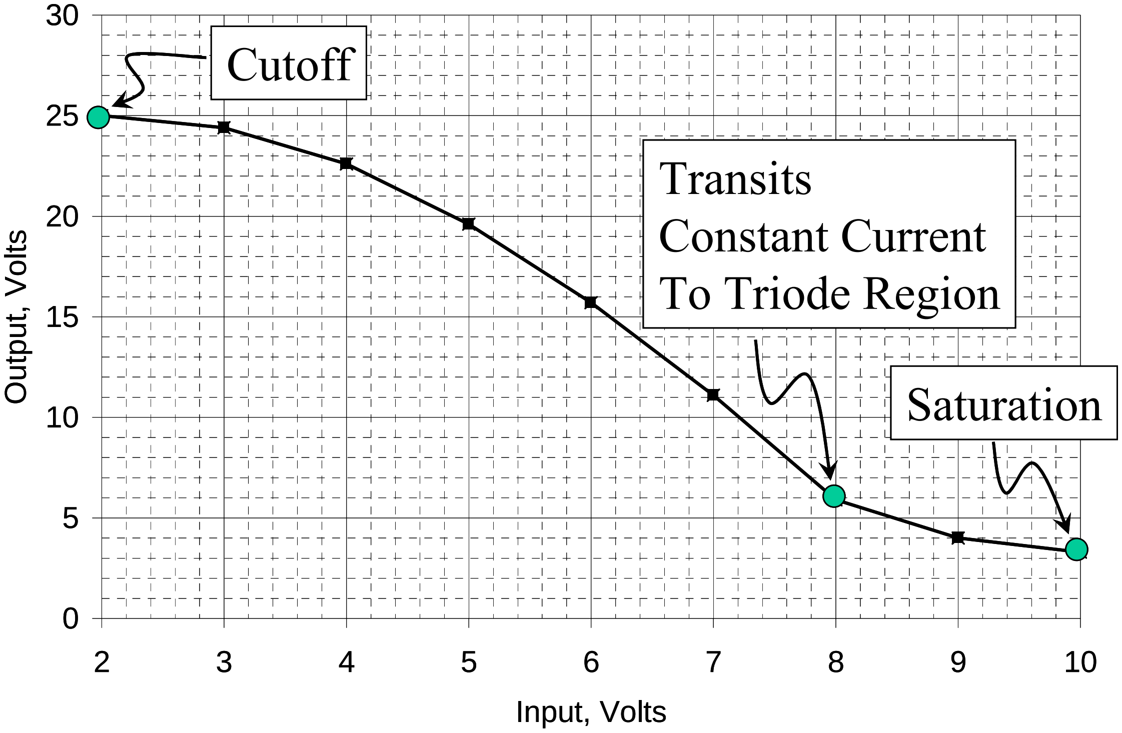

Figure 6. Input-Output Characteristic Curve for Figure 4.

The cutoff point is where the gate voltage is equal to the threshold voltage, $v_G = V_{TR}$, and is marked on Figure 6. The load line crosses the boundary between the constant current region and the triode region at a gate voltage of eight volts, and this point is marked on the curve. Note that the square law shape of the drain current versus gate voltage curve is apparent in the constant current region. The saturation point is where the gate voltage is high enough to have very little effect on the drain current, and that is at about 10 Volts and above, and this is marked on the plot.

Looking at the input-output characteristic curve that we have drawn as Figure 6, the effective output voltage range is about 5 Volts to 25 Volts. The curve is not linear, so a sine wave input will not produce an accurate sine wave output – the output at the drain will have distortion relative to the input at the gate. This can be reduced to acceptable levels with circuit feedback as is often done in audio power circuits.

Special essay response. Audio enthusiasts and others may have interest in this circuit but some concepts are out of scope of Electronics I; thus this is for your interest and future study, but is not graded as part of the Final Examination.

The maximum continuous sine wave power across a resistive load is the peak to peak voltage, squared, divided by 8 times the resistance of the load. For a peak-to-peak voltage of 20 Volts and a resistive load of 0.5 Ohms, this is 100 Watts. A transformer that is capable of handling this power and voltage level, with a turns ratio of one to $\sqrt{4/0.5}$, or 1:2.8, can present a load of 0.5 Ohms to the circuit from its primary winding with a load of 4 Ohms on the secondary winding. The inductance on the primary must be significantly higher than 0.5 Ohms at the lowest frequency that the amplifier is expected to perform.

Problem 4 (25%)

For a bipolar junction transistor (BJT) in the circuit of Figure 7 with v-i curves as shown in Figure 8, we have a collector load resistor with a resistance of $1\,k\Omega$, and a resistor in series with the base with resistance $100\,k\Omega$. The voltage drop from base to emitter is 0.7 Volts.

- Draw the load line on Figure 8.
- Complete Table 2 below by computing the base current from each input voltage v_{IN}, selecting the transistor v-i curve from the base current, and reading the output voltage as the intersection of that v-i curve with the load line.
- Draw a plot of output voltage (y axis) versus input voltage (x axis).

Table 2. Input Voltage, Base Current, and Output Voltage from Load Line.

v_{IN}	i_B	v_{OUT}
0.7 Volts	0 μA	20 Volts
1.7 Volts	10 μA	16 Volts
2.7 Volts	20 μA	12.2 Volts
3.7 Volts	30 μA	8.6 Volts
4.7 Volts	40 μA	5.3 Volts
5.7 Volts	50 μA	2.1 Volts
6.7 Volts	60 μA	0.84 Volts

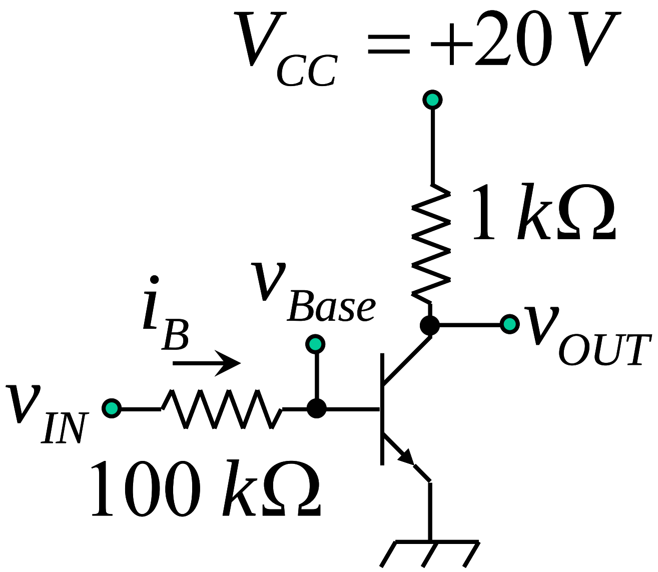

Figure 7. Simple BJT inverter circuit for Problem 4.

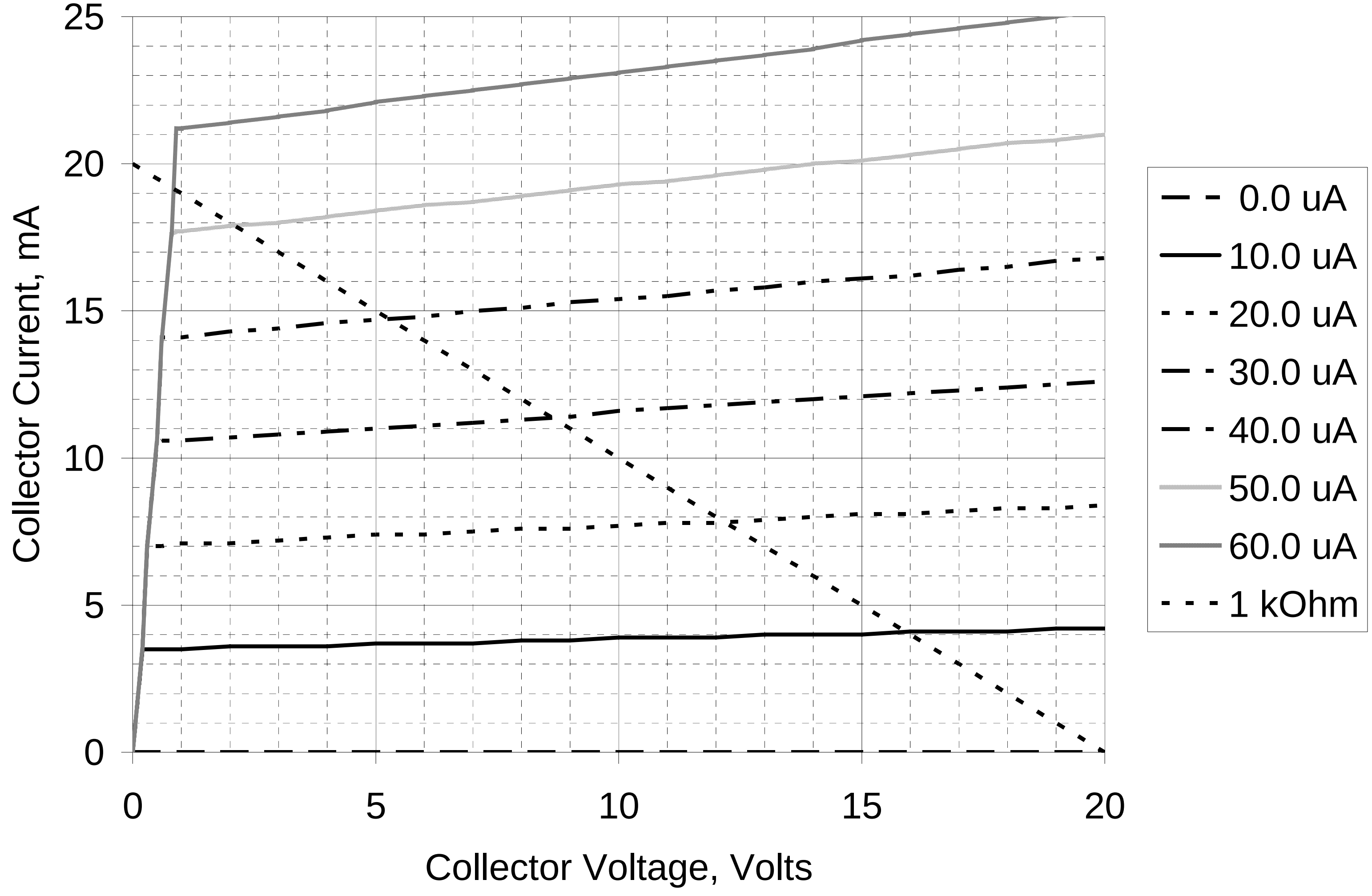

Figure 8. BJT v-i Curves.

Solution

The load line is drawn in Figure 8. We can complete the second column of Table 2 using Ohm's law and noting that, since we are given the base-emitter drop of 0.7 Volts in the problem statement and the emitter is grounded in the circuit given in Figure 7, the base voltage is always 0.7 Volts and the voltage across the 100 kOhm resistor is $\left(v_{IN} - 0.7 \text{ Volts}\right)$. The entries in the second column of Table 2 tell us which v-i curve to intersect with the load line to obtain the output voltage for that row of the table. This was done to flesh out Table 2 as required in the problem statement. The first and last columns of the table are used to provide the input-output characteristic curve shown below as Figure 9.

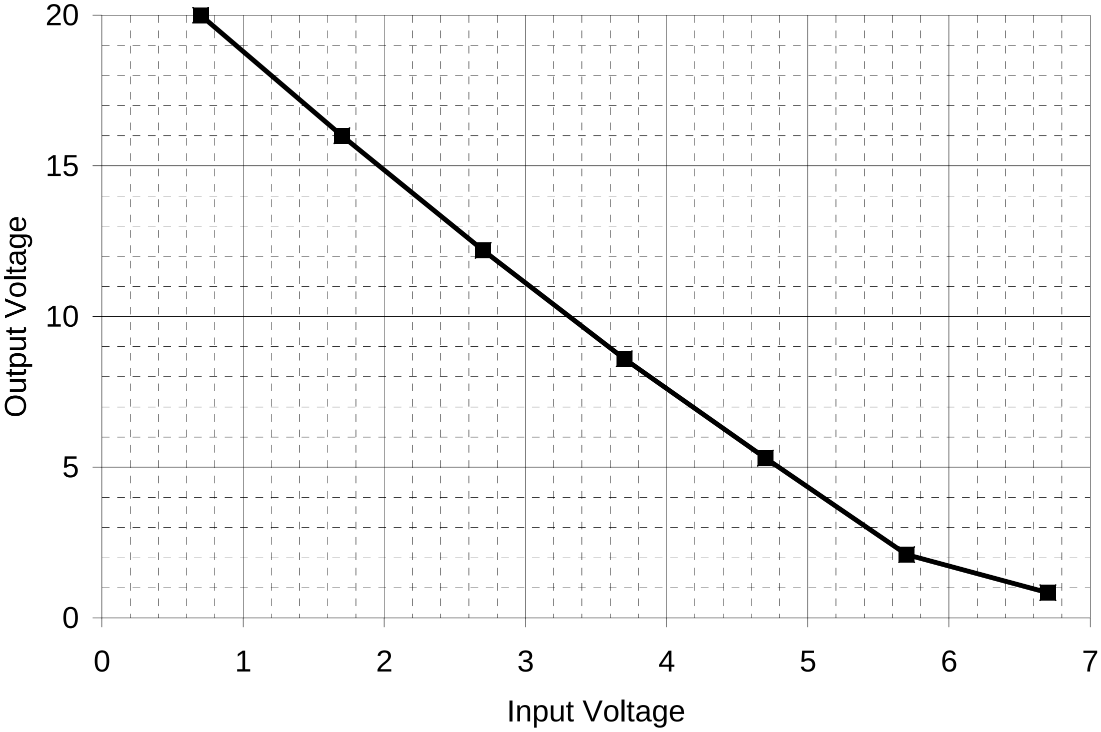

Figure 9. Output Voltage vs. Input Voltage for Problem 4.