IGFET Transistors

Biasing, Gain, Input and Output

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1 Introduction

We begin with the concept of an insulated gate field-effect transistor (IGFET). This class of transistor is usually referred to as a metal oxide semiconductor field-effect transistor (MOSFET), which is the earliest and still the most common type, although insulation types other than metal oxide are sometimes used so that IGFET is more accurate than MOSFET for some devices.

We begin with the inverting amplifier configuration, with a source resistor and the gate bias provided by a voltage divider from the main supply voltage. The goal is to understand and design an amplifier for maximum voltage swing on output, or for small signal with minimum power or lowest noise.

We use one model for our biasing analysis and a separate model for our signal model. Our biasing analysis model is a simple constant voltage drop for the gate-source junction. The *h-parameter* value of input resistance is used with the signal model but not with the bias model. The *h-parameter* gate-drain current gain is used in both the biasing analysis and signal models. The *h-parameter* drain resistance is neglected here in both models, as is the drain-gate feedback coupling coefficient.

Our biasing analysis begins with the use Kirchhoff's laws[1] to solve the bias model. The load line is presented and we include here the concept of the use of the drain and source resistors to limit transistor power dissipation. The bias circuit analysis concludes with the Thévenin equivalent circuits for the three transistor terminals

The signal analysis uses a different model that omits DC voltage sources and includes the gate terminal input resistance. Input and output capacitive coupling is also included in the signal model.

We conclude with a section on design of MOSFET inverting amplifiers. This analysis begins with simplification of the equations developed from the biasing and signal models by looking at the engineering approximations, and the design constraints required to support the accuracy and usefulness of these approximations. Then these approximations are used in a simple step-by-step process of designing a robust MOSFET amplifier in an inverting configuration.

The source follower is supported by the models and analyses prepared for the inverting amplifier. The biasing and design of a robust source follower concludes the design section.

2 Types of IGFET

There are several types of insulated gate field-effect transistors (IGFETs) in common use. The early term metal oxide semiconductor field-effect transistor (MOSFET) is still in use, and MOSFET is usually acceptable as a generic term for IGFETs. The metal oxide, and the insulation in the IGFET, is the insulating material between the gate terminal and the substrate between the source and drain terminals. This insulator must have very low leakage, of course, but another requirement for good performance of the transistor is that the dielectric constant of the material must be very high. The first IGFET technology

used a layer of metal oxide that could be formed as a logical step in the fabrication process. Techniques have been developed that can apply layers of sapphire and other materials as the insulator that improve MOS in insulation resistance, peak voltage without breakdown, and dielectric constant.

Junction field-effect transistors (JFETs) are, strictly speaking, not IGFETs because the gate terminal is separated from the substrate by the depleted region of a semiconductor, and the gate is connected to the substrate across this reverse-biased junction. However, JFETs can be analyzed using the techniques in this report, as modified as appropriate by noting that the saturation current of this diode does exist and that the gate terminal is not truly insulated. JFETs are always depletion mode FETs because the junction must be reverse biased, so the transition voltage for JFETs is always negative.

3 Drain Current as a Function of Gate and Collector Voltages

3.1 The linear region

The MOSFET is similar in some ways to a BJT, and a strong analogy exists between the terminals. The MOSFET gate terminal is analogous to the BJT base terminal, the MOSFET source terminal is analogous to the BJT emitter terminal, and the MOSFET drain terminal is analogous to the BJT collector terminal.

The basic physics of a MOSFET is divided into three regions[2]: cutoff, when essentially no drain current flows, the triode region, in which the gate voltage exceeds the threshold voltage but the drain voltage is low and the drain current is a significant function of the drain voltage, and the constant current region, in which the drain voltage is sufficiently high that the drain current no longer increases with drain voltage. These regions are determined by the gate-source potential V_{GS}, the threshold gate-source potential V_T and the drain-source potential V_{DS}. The conditions for each region are:

$$\begin{cases} \text{Cutoff:} & V_{GS} \le V_T \\ \text{Triode:} & V_{DS} \le V_{GS} - V_T \\ \text{Constant current:} & V_{DS} > V_{GS} - V_T \ . \end{cases} \tag{3.1}$$

In the triode region, the drain current is expressed as a function of the gate-source potential and the drain-source potential by[3]

$$I_D = K \cdot \left(2 \cdot \left(V_{GS} - V_{TR}\right) \cdot V_{DS} - V_{DS}^2\right) \cdot \left(1 + \frac{V_{DS}}{V_A}\right) \ \left(\text{Triode region}\right) \tag{3.2}$$

where

(3.3)
$$\begin{cases} K = \text{Conductance parameter} \\ V_A = \text{Early voltage} \\ V_{GS} = \text{Gate-source voltage} \\ V_{TR} = \text{Transition voltage} \\ V_{DS} = \text{Drain-source voltage.} \end{cases}$$

In the constant current region, the drain current follows the equation[4]

(3.4)
$$I_D = K \cdot \left(V_{GS} - V_{TR}\right)^2 \cdot \left(1 + \frac{V_{DS}}{V_A}\right) \ \left(\text{Constant current region}\right).$$

The voltage V_A is the point on the horizontal axis of the v-i curves where all the constant current region lines meet. This value is typically 100 Volts for a MOSFET but can vary from 35 Volts to 1,000 Volts or more. Sometimes this parameter is called the *channel length modulation factor* and is denoted by λ,

(3.5)
$$\lambda = \frac{1}{V_A}.$$

The dynamic conductance at the drain of a MOSFET is the slope of the v-i curve in the constant current region, and is found as the derivative of (3.4) with respect to V_{DS},

(3.6)
$$G_D = \frac{K \cdot \left(V_{GS} - V_{TR}\right)^2}{V_A} \approx \frac{I_D}{V_A}.$$

For our small signal model, we are required to find the transconductance at a given operating point. This is found as the derivative of (3.4) with respect to V_{GS},

(3.7)
$$g = 2 \cdot K \cdot \left(V_{GS} - V_{TR}\right) \cdot \left(1 + \frac{V_{DS}}{V_A}\right) = \frac{2 \cdot I_D}{V_{GS} - V_{TR}}.$$

The v-i curves for a MOSFET with a conductance parameter *K* of 1 mA/V^2, a transition voltage of 2 Volts, and an Early voltage of 2 Volts, is shown below in Figure 1 for gate voltages varying from 2 Volts, the transition voltage, to 8 Volts. A dotted line separates the triode region and the constant current region, where the drain current is nearly constant.

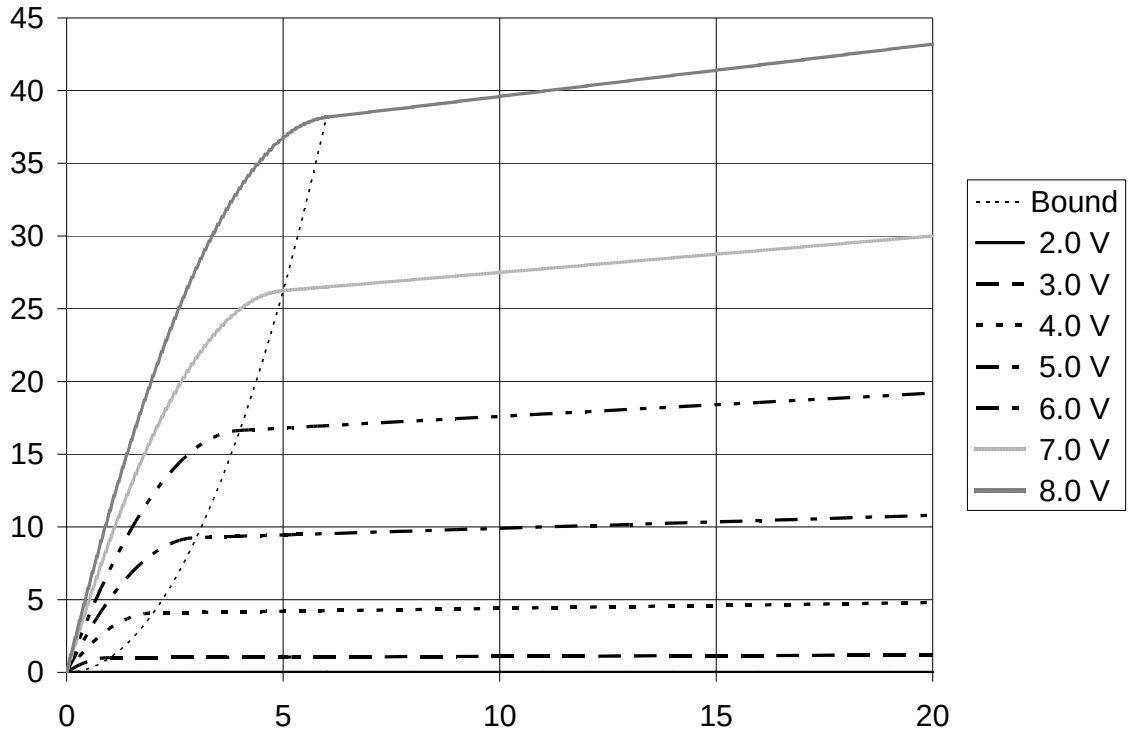

Figure 1. Representative v-i curves for an IGFET, illustrating the operating regions.

3.2 Off and On Regions

The off region is essentially elementary. The on region requires us to understand the output conductance in the triode region. This is the reciprocal of the on resistance, and is found as the derivative of (3.2) with respect to V_{DS},

$$G_{ON} = 2 \cdot K \cdot \left(V_{Gs} - V_{TR} - V_{DS}\right) \cdot \left(1 + \frac{V_{DS}}{V_A}\right) + \frac{K \cdot \left(2 \cdot \left(V_{GS} - V_{TR}\right)^2 - V_{DS}^2\right)}{V_A} \approx 2 \cdot K \cdot \left(V_{GS} - V_{TR}\right). \tag{3.8}$$

This is similar in magnitude to the transconductance equation for the linear region, but the on condition for switching applications will have a far higher gate voltage drive than a transistor in the linear region.

4 The Load Line

4.1 Drawing the Load Line

The load line is a straight line on a set of transistor drain-source v-i curves that reflects the Thévenin equivalent circuit made up of the supply voltage V_{CC} and the drain and source circuit resistance $\left(R_C + R_E\right)$. Figure 2 shows a load line on a typical NPN MOSFET transistor. The load line intercepts the voltage axis at V_{CC} and the current axis at $V_{CC}/\left(R_C + R_E\right)$. The transistor can operate as a linear amplifier only when the operating point is on the load line in a region between saturation and cutoff, with operation in the constant current region, to the right of the dotted line labeled "Bound," preferred.

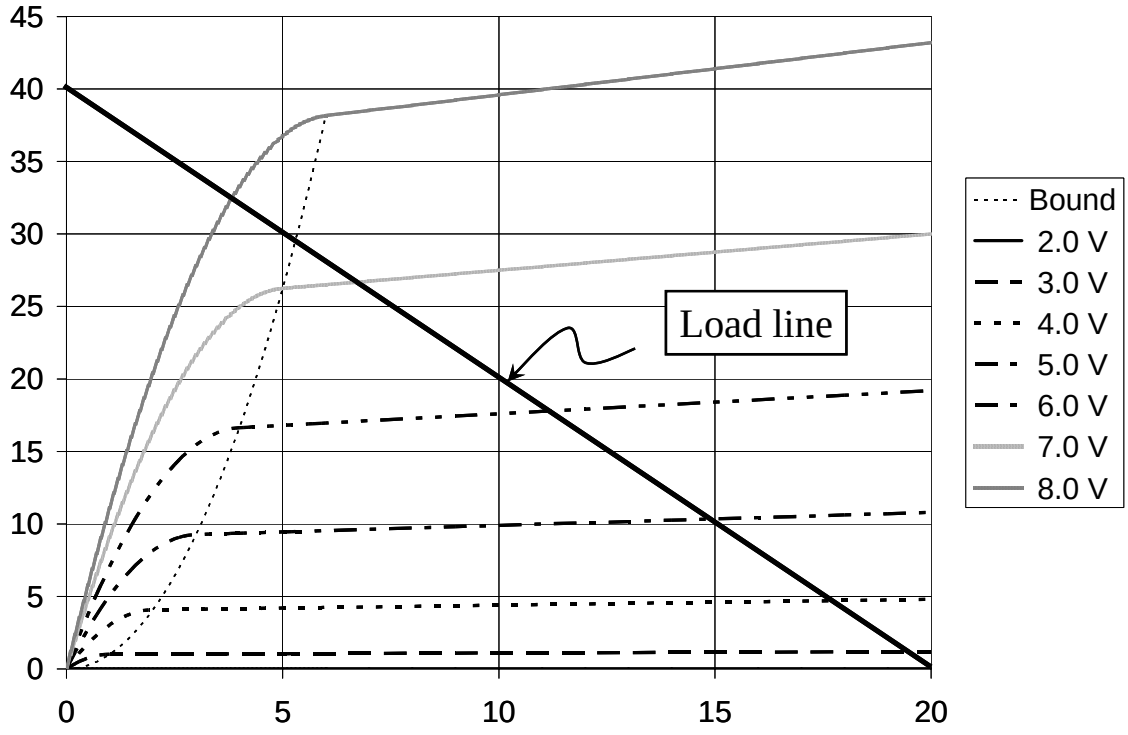

Figure 2. Idealized v-i Curve and Load Line for a MOSFET.

4.2 Controlling the Power Dissipated in the IGFET

An important addition to the load line is a curve of allowable power dissipation for the transistor. This is a hyperbola on the v-i curve with asymptotes of the v and i axes. The region between this curve and the axes represents the allowable operation region of the transistor, where the power dissipated does not exceed the maximum allowed. The equation for the allowed region is

(4.1) $$V_{CE} \cdot i_C < P_{MAX} .$$

The load line can cross the hyperbola and part of it may be outside the allowed region. But, the zero-signal operating point must be inside the allowed region.

The value of the drain resistor R_C plus that of the source resistor R_E can be defined to limit the maximum possible power available to the transistor. We know by maximum power transfer principles that this power is

$$PMAX_{Transistor} = \frac{V_{CC}^2}{4 \cdot (R_C + R_E)} \tag{4.2}$$

so we can ensure that the maximum power dissipated by a transistor will never exceed a specified maximum by limiting R_C according to

$$R_C + R_E \geq \frac{V_{CC}^2}{4 \cdot P_{MAX}} . \tag{4.3}$$

5 Simplified Equivalent Circuits

We will consider a bipolar junction transistor (MOSFET) in an inverting amplifier configuration, which is biased according to the feedback-bias circuit[5] given below as Figure 3.

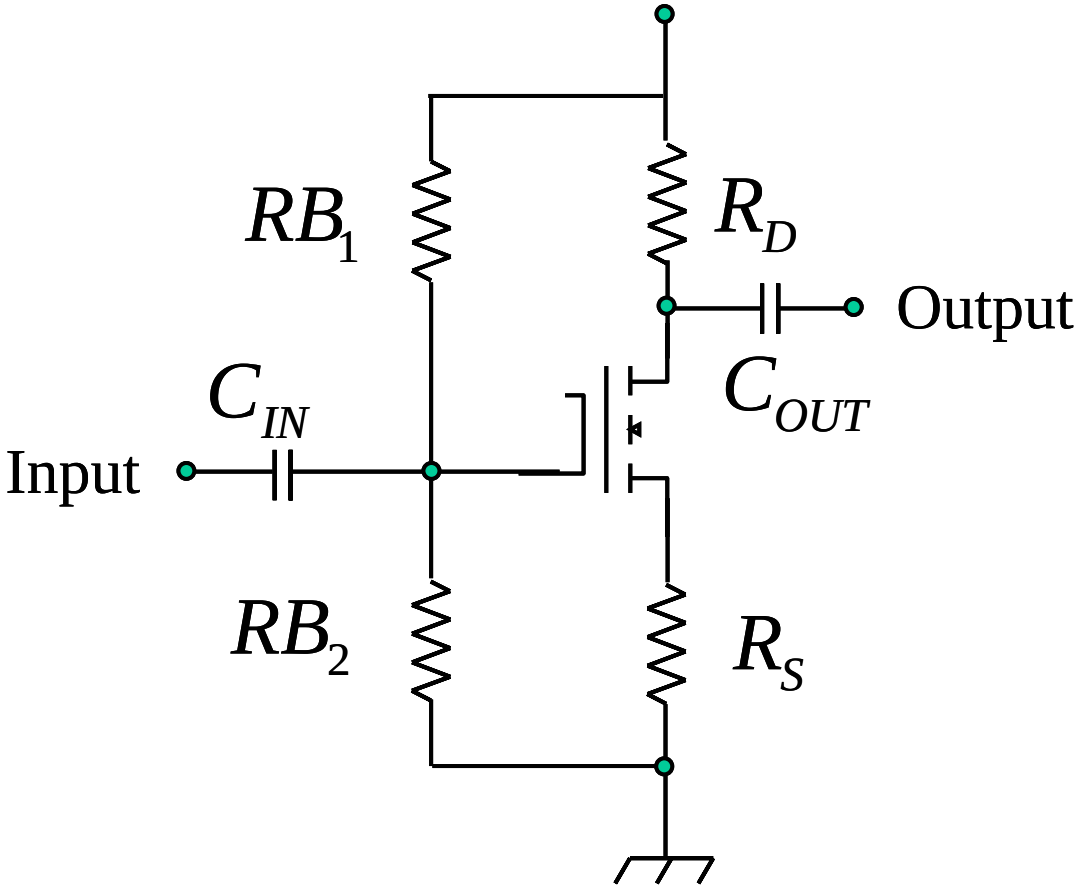

Figure 3. MOSFET in Inverting Amplifier Circuit with Bias Circuitry.

This is the configuration most often used for MOSFET amplifiers in either the inverting amplifier or source follower configuration. Most analysis that follows is directed to the inverting amplifier but we have a short section on the source follower, which is obtained from the circuit of Figure 3 simply by taking the value of the drain load resistor R_C as zero and obtaining the output from the source terminal.

The circuit shown in Figure 4 is a simplified model of MOSFET. The portion of the circuit inside the doted rectangle is a Thévenin equivalent circuit of the biasing circuitry, not the actual biasing circuit. The gate, source, and drain terminals are denoted by B, E and C respectively. The gate-source diode junction is modeled by a constant voltage drop, shown in Figure 4 as the source V_{BE}, which for most silicon transistors is about 0.7 Volts.

This is simpler than the *h parameter* model used in SPICE and other detailed models. The intent here is to provide a simple analysis and design method that enables design of robust MOSFET inverting amplifiers and source followers from data sheet parameters without additional computer models.

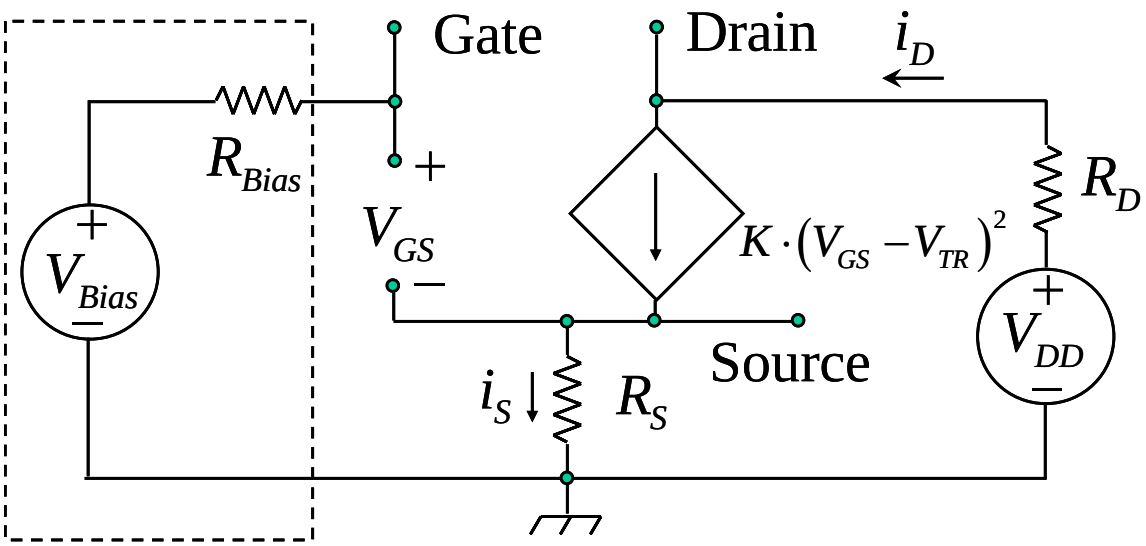

Figure 4. Simple Large Signal Model of MOSFET Inverting Amplifier with Feedback Bias Circuit.

The circuit of Figure 4 is similar to those considered in Example 1.3, pages 10-12, and homework problem 1.65 (a) on page 33. The principal difference is that the transistor model in Figure 4 models the gate-source junction as a voltage drop rather than a resistance. Note that for most MOSFETs in normal operation, the gate current is zero, and for JFETS it is only the reverse current of a diode.

5.1 Setting the Operation Point with the Large Signal Equivalent Circuit

5.1.1 Solution given a desired operating point

To solve for the bias circuit algebraically, we need the values of the conductance parameter K and the threshold voltage V_{TR}. These can be measured for individual devices by connecting the MOSFET in a source follower configuration as shown in Figure 5 below. Use a value of V_{CC} near or equal to that to be used in your amplifier circuit. Adjust the gate voltage to obtain a source voltage of about 1 Volt; this will set the drain current to about 10 μA, a very small value. For a source resistor R_S of about100 $k\Omega$, the threshold voltage is measured as the difference between V_G and V_S. Then, change the source resistor R_S to 1 $k\Omega$ and increase V_G to slightly less than $V_{DD} - V_{TR}$ to get the drain current as high as possible while operating in the constant current region. The drain current is found from the source voltage V_S and the source resistor R_S using Ohm's law and the conductance parameter K is found from

(5.1)
$$K = \frac{i_D}{\left(V_G - V_S - V_{TR}\right)^2}.$$

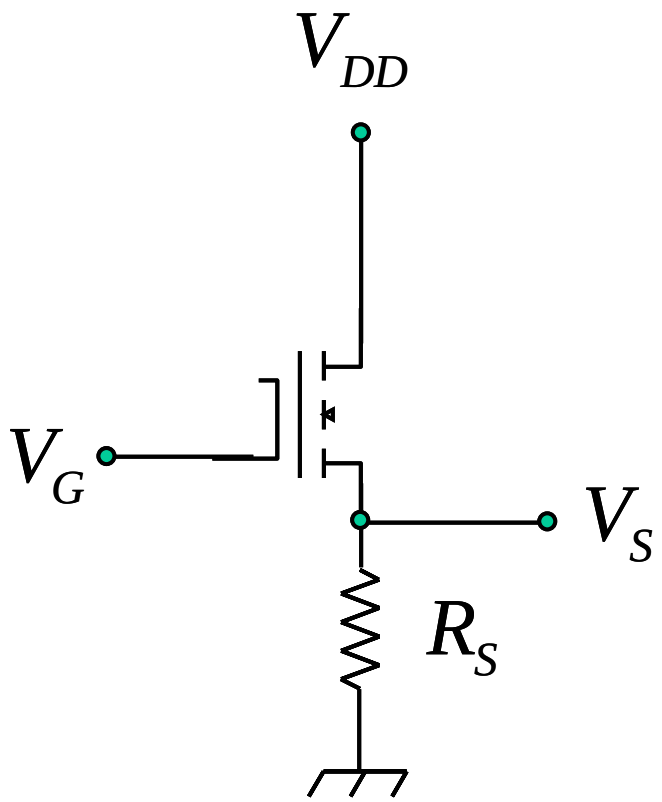

Figure 5. Source follower circuit for measuring MOSFET parameters.

The circuit of Figure 4 is very simple to solve in spite of the fact that the controlled source is not linear. If we specify the drain voltage, we specify the drain current, and we have

(5.2) $$i_D = K \cdot \left(V_{GS} - V_{TR}\right)^2$$

and

(5.3) $$V_S = i_D \cdot R_S$$

or,

(5.4) $$V_G - V_{TR} = \sqrt{\frac{i_D}{K}} + i_D \cdot R_S \,.$$

Since there is no gate current, the gate voltage is equal to the bias voltage and we can set the voltage divider formed by RB_1 and RB_2 to provide the correct bias.

5.1.2 Bias solution using engineering approximations

We may need to do at least a first-cut bias circuit using engineering approximations because the value of the conductance parameter K may not be known accurately or at all because we are designing for all transistors of a given type as opposed to a single specific transistor, and the threshold voltage V_{TR} may similarly not be known. We know that the source voltage V_S will be equal to the gate voltage V_G minus the threshold voltage V_{TR}, minus whatever is required to provide enough current from the controlled current source to form a voltage drop across R_S. So, we estimate a value of the threshold voltage V_{TR} from the data sheet of the transistor and set the bias voltage to the desired source voltage plus V_{TR}, plus a margin to allow for the MOSFET.

5.2 Solving the Signal Model

5.2.1 The Signal Equivalent Circuit

The signal equivalent circuit is shown in Figure 6. take the transconductance from (3.7) to define the controlled source for the small signal model. As with the large signal circuit, the small signal circuit is very simple to solve. Looking at the source as a current node and applying Kirchhoff's current law, we see that the gate current is zero and that the source current i_S, defined as positive out of the transistor terminal, is equal to the drain current. Thus we have only one unknown current, the drain current i_D, and that current is driven by the controlled source. From Ohm's law we have

(5.5) $$v_S = g \cdot \left(v_G - v_S\right) \cdot R_S$$

which immediately provides a solution for the source voltage,

(5.6) $$v_S = \frac{g \cdot R_S}{1 + g \cdot R_S} \cdot v_G \,.$$

Ohm's law gives us the source and drain current,

(5.7) $$i_S = i_D = \frac{g}{1 + g \cdot R_S} \cdot v_G$$

from which we again use Ohm's law to obtain the drain voltage:

(5.8) $$v_D = -\frac{g \cdot R_D}{1 + g \cdot R_S} \cdot v_G .$$

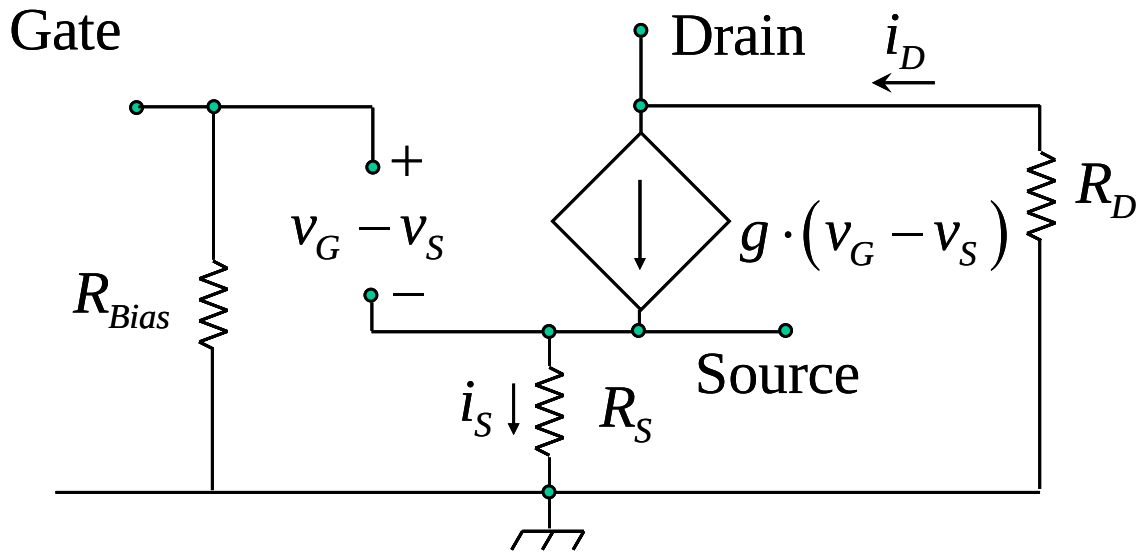

Figure 6. Signal Model of Circuit of Figure 1.

5.2.2 The Equivalent Gate Resistance

The gate resistance is simply the parallel combination of the bias voltage divider resistors RB_1 and RB_2 in Figure 3.

5.2.3 Thévenin Equivalent Circuits for the Drain and Source

The Thévenin equivalent impedance for the drain is very simple; the Thévenin equivalent resistance is R_D and the open circuit voltage is given by (5.8).

The Thévenin equivalent circuit for the source is almost as simple. The open circuit voltage is given by (5.6). The short circuit current is found by noting that, for a source shorted to ground, v_S is zero in the equation for the controlled source in Figure 6, and the short circuit current for the source terminal is

(5.9) $$i_{S,SC} = g \cdot v_G$$

so that the Thévenin resistance at the source is

(5.10) $$RS_{Th} = \frac{v_{S,OC}}{i_{S,SC}} = \frac{\frac{g \cdot R_S}{1 + g \cdot R_S} \cdot v_G}{g \cdot v_G} = \frac{R_S}{1 + g \cdot R_S}$$

6 Designing for Robustness with Variations in Transistor Parameters

6.1 Summary of gain and Thévenin equivalents

The base requirement for the biasing and feedback resistors to control the circuit and provide robustness is

(6.1) $$g \cdot R_S \gg 1.$$

Given (6.1), the gain of the source follower is very nearly unity and the gain of the inverting amplifier is

(6.2) $$Gain_{INV} \approx -\frac{R_D}{R_S}.$$

The Thévenin resistance seen at the output of a source follower is

(6.3) $$R_{S,Th} \approx \frac{1}{g}.$$

6.2 Step by Step Design Process

7 Conclusions

The use of MOSFET transistors in inverting amplifiers is supported by the simple robust circuit shown in Figure 3. The design is similar to that of an inverting amplifier in an op-amp, with the drain resistor R_D taking the place of the inverting amplifier feedback resistor and the source resistor R_S taking the place of the input resistor, so that the gain is

(7.1) $$G = -\frac{R_D}{R_S}.$$

Unlike the op-amp inverting amplifier, the input impedance of the inverting amplifier is high relative to R_S, and is simply R_{Bias}, the parallel combination of the voltage divider resistors RB_1 and RB_2, which can be very high.

Although the high resistances used by some op-amps may compensate for this impedance buffering effect, the MOSFET inverting amplifier is capable of very high performance with a very simple circuit. For AC coupled signal amplifiers, the MOSFET inverting amplifier is a good choice because of its simplicity relative to op-amp circuits, particularly if high gain-bandwidth product is required.

The process given in Section 5.1 provides a robust design using data sheet numbers, and can be completed without models such as SPICE, and provides uniform performance for normal variation in transistor performance parameters such conductance parameter K or threshold voltage V_{TR}.

8 References

[1] *Introduction to Electric Circuits*, 7th Edition, Richard C. Dorf and James A. Svoboda, ISBN 0-471-73042-4
[2] *Microelectronic Circuits and Devices*, 2nd Edition, Mark N. Horenstein, Prentice-Hall (1996), ISBN 0-13-701335-3, Section 5.2.
[3] Horenstein, loc. cit., equations (5.4) page 245 and (5.7) page 246, discussion in section 5.4.1 pp 273-274.
[4] Horenstein, loc. cit., equation (5.7) page 246 and discussion in section 5.4.1 pp 273-274.
[5]Horenstein, loc. cit.; see Example 7.4 pp 403-405.