FINAL EXAMINATION SOLUTIONS

Electronics I for ECE
Course Number ECE 09-311 1
CRN 20460

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Problem 1 (20%)

Refer to the circuit of Figure 1. Use the steady-state sine wave solutions and the concepts of inductive and capacitive impedance, and apply circuit theory to solve the problems much as you would with resistive networks. Show all work and provide equations for the following:

1. Show the complex form $vz_{IN}(t)$ for the input voltage such that $v_{IN}(t)$ is the real part of $vz_{IN}(t)$ and $vz_{IN}(t)$ has constant complex amplitude with time.
2. Derive and show the voltage across the resistor R in either real or complex format..
3. Provide the complex voltage transfer function $G(\omega)$ that, when multiplied by $vz_{IN}(t)$, yields the complex form of the output voltage across the resistor R.

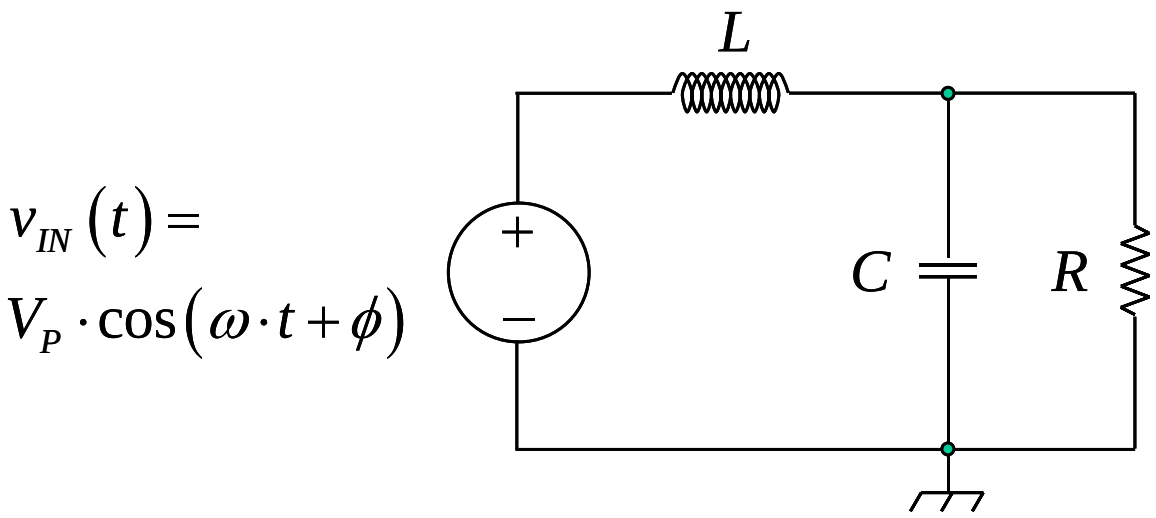

Figure 1. Circuit to Solve for Problem 1.

Solution

The base equations are

$$\text{(1.1)} \qquad \begin{cases} vz_{IN}(t) = V_P \cdot \exp\left(j \cdot (\omega \cdot t + \phi)\right) \\ Z_L = j \cdot \omega \cdot L \\ Z_C = \dfrac{1}{j \cdot \omega \cdot C} \end{cases}$$

The voltage across R is found by the voltage divider equation. The impedance of the resistance in parallel with the capacitance is

$$\text{(1.2)} \qquad \frac{1}{Z_{RC}} = \frac{1}{R} + \frac{1}{Z_C} = \frac{1}{R} + j \cdot \omega \cdot C = \frac{1 + j \cdot \omega \cdot R \cdot C}{R}$$

so we have the voltage across R as

$$vz_R(t) = \frac{Z_{RC}}{Z_L + Z_{RC}} \cdot vz_{IN}(t)$$

$$= \frac{\frac{R}{1 + j \cdot \omega \cdot R \cdot C}}{j \cdot \omega \cdot L + \frac{R}{1 + j \cdot \omega \cdot R \cdot C}} \cdot vz_{IN}(t) \qquad (1.3)$$

$$= \frac{1}{1 + j \cdot \omega \cdot \frac{L}{R} - \omega^2 \cdot L \cdot C} \cdot vz_{IN}(t)$$

The transfer function $G(\omega)$ is found as

$$G(\omega) = \frac{vz_{OUT}(t)}{vz_{IN}(t)} = \frac{1}{1 + j \cdot \omega \cdot \frac{L}{R} - \omega^2 \cdot L \cdot C}. \qquad (1.4)$$

Problem 2 (20%)

Figure 2 below is a simple model of the IRFZ24N MOSFET from IRC that offers a reasonable approximation of the v-i curves in the IRC data sheet for an ambient temperature of 25 C. (Continued on next page)

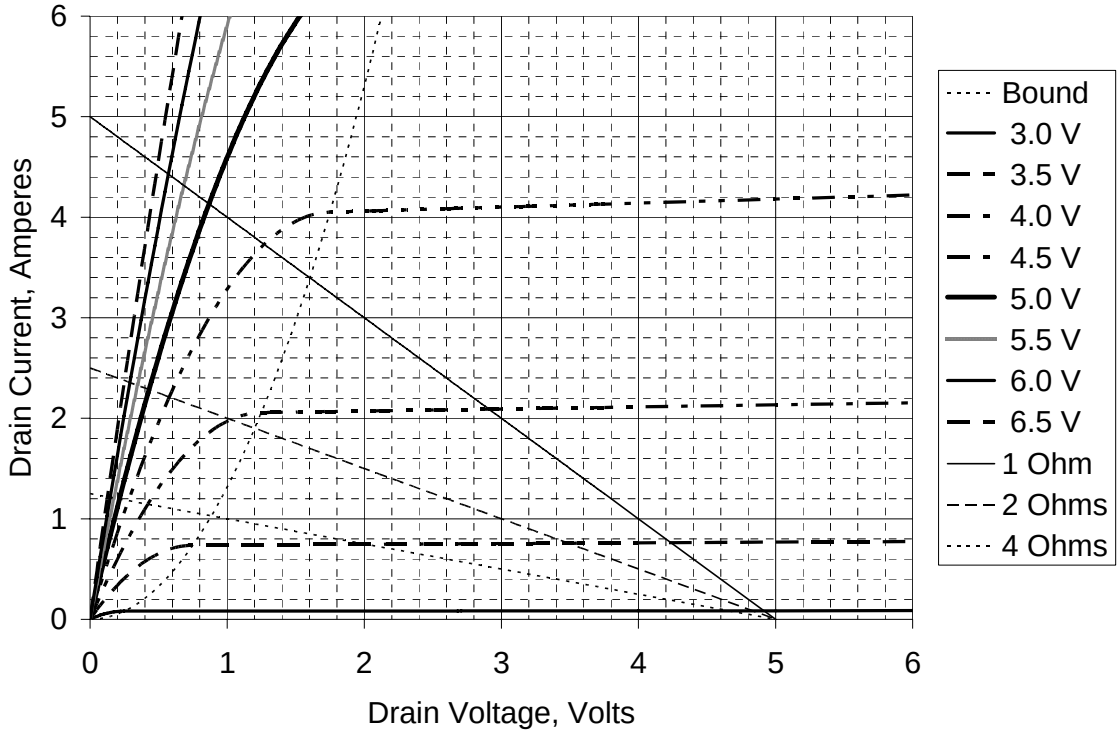

Figure 2. V-i Curves from a Model of the IRFZ24N MOSFET.

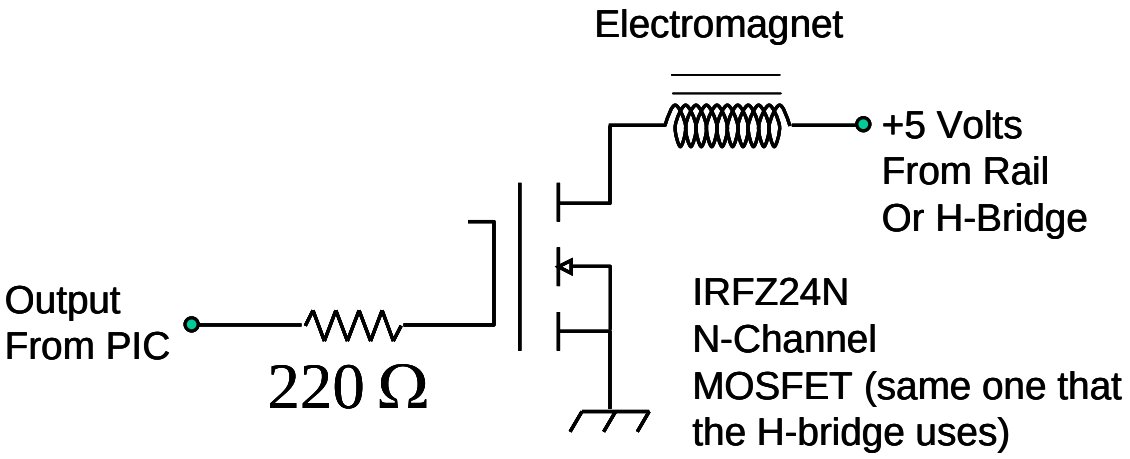

Figure 3. Microcontroller Operated Electromagnet Driver from 5 Volts Using the IRFZ24N MOSFET

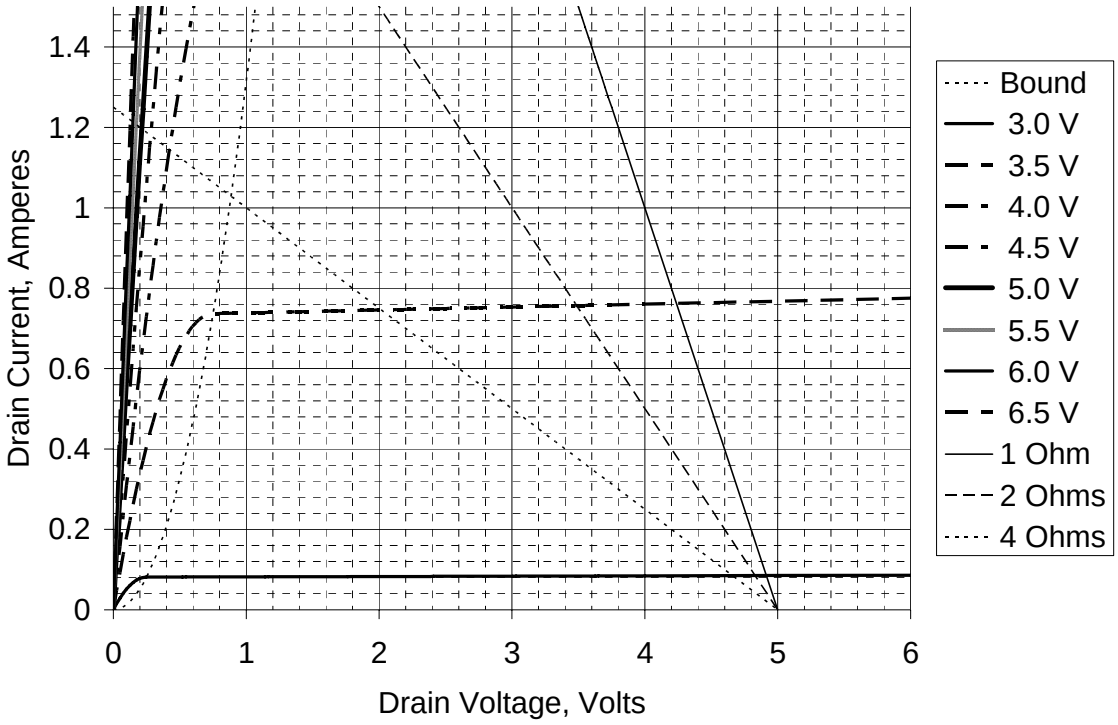

Figure 4. Expanded v-i Curves from a Model of the IRFZ24N MOSFET.

The transition voltage V_{TR} for this model is 2.75 Volts. Figure 4 above is another set of v-i curves from the model of the IRFZ24N MOSFET that zooms in on the lower drain currents.

Consider the electromagnet a simple resistive load. Assume that the PIC microcontroller provides 5.0 Volts of drive for the MOSFET gate. Draw the load lines for electromagnet resistances of 1 Ohm, 2 Ohms, and 4 Ohms. Give the steady-state DC current through the electromagnet for each resistance. Compare that current with the current that would be produced by 5 Volts across the electromagnet.

Solution

The load lines are drawn on the figures. The results from the intersection of the load lines with the MOSFET v-i curves for 5 Volts gate voltage are as shown below in Table 1.

Table 1. Comparison of Load Line and Direct Connection Currents

Resistance	Load Line Current	Straight Connection Current
1 Ohm	4.14 Amperes	5.0 Amperes
2 Ohms	2.28 Amperes	2.5 Amperes
4 Ohms	1.20 Amperes	1.25 Amperes

Problem 3 (20%)

See Figure 5 below for the circuit to analyze for this problem. Use the perfect op-amp approximations to analyze the circuit.

- Solve for e_{OUT} in terms of e_1 and e_2.
- Simplify and interpret the result for the special case
$$\frac{R_1 \cdot R_3}{R_2 \cdot R_4} = 1.$$
- What is the input impedance as seen at e_1 and e_2? What is the Thévenin equivalent for the output at e_{OUT}?

HINT: Use superposition to analyze each op-amp. Find e_x in terms of e_2, and find e_{OUT} in terms of e_1 and e_x separately, then add the results and substitute your solution for e_x in terms of e_2.

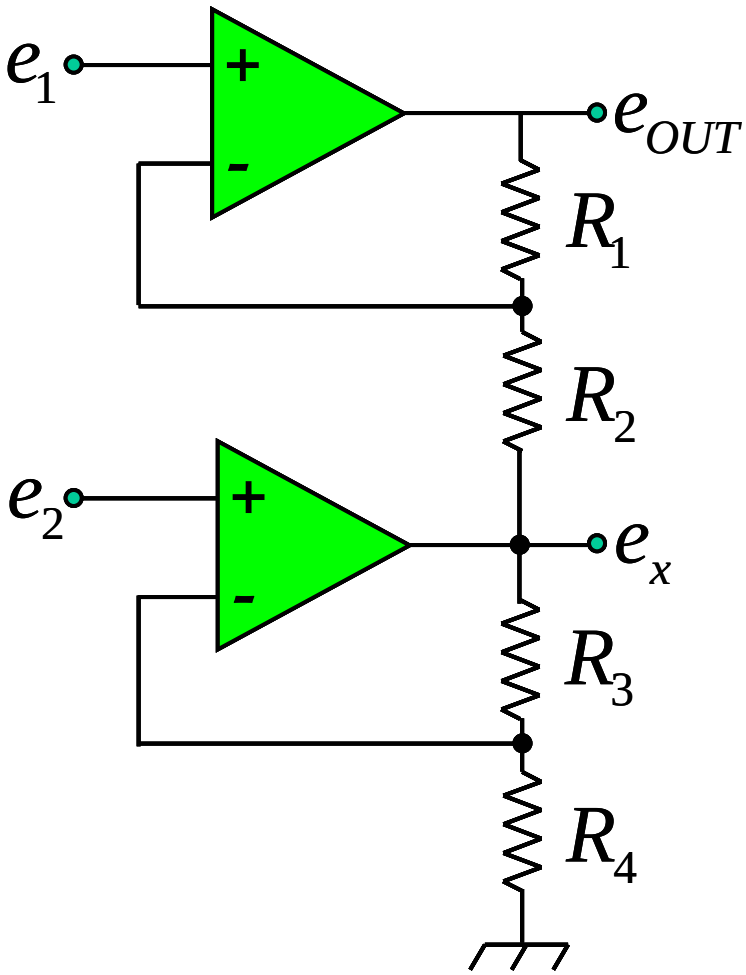

Figure 5. Op-amp circuit for Problem 3.

Solution

Except for some capacitive coupling, this is the same op-amp configuration that is used in the Term Project. In Laboratory 3, you were asked to build this circuit and test it. In the laboratory report instructions, you were asked to analyze this circuit for your lab report. See this link for the lab protocol:
http://rowan.jkbeard.com/Electronics_I_ECE_Materials/2007-02-23_Electronics_I_Lab_03.htm

We are instructed to use the perfect op-amp approximation, which is infinite input impedance, voltage source output, and infinite gain. We will use the hint and fine e_x first. Note that the bottom op-amp in Figure 5 is a non-inverting amplifier. Because this is a perfect op-amp and has a voltage source output, any current flowing through R_2 will have no effect on e_x, so we see that we can analyze this non-inverting amplifier while ignoring the rest of the circuit. We can analyze this circuit in detail or simply use what we have learned studying non-inverting amplifiers – and went over in the Study Session on April 30 – and write e_x as

(3.1) $$e_x = \left(1+\frac{R_3}{R_4}\right)\cdot e_2 .$$

The hint next tells us to look at e_{OUT} as a function of e_1 and e_2 separately using the principle of superposition - taking one of the inputs as zero volts and finding the output due to the other, then using the principle of linearity by taking the output as the sum of the outputs due to all of the inputs separately. From the input e_x and taking e_1 as zero, we see that we have a simple inverting amplifier,

(3.2) $$e_{OUT}\left(e_x\right) = -\frac{R_1}{R_2}\cdot e_x .$$

Conversely, taking e_x as zero, we see that we again have a simple non-inverting amplifier, and.

(3.3) $$e_{OUT}\left(e_x\right) = \left(1+\frac{R_1}{R_2}\right)\cdot e_1 .$$

As the hint suggests, we add the two results from (3.2) and (3.3),

(3.4) $$e_{OUT} = \left(1+\frac{R_1}{R_2}\right)\cdot e_1 - \frac{R_1}{R_2}\cdot e_x .$$

Since we have e_x as a function of e_2 from (3.1), which, as suggested by the hint, we substitute into (3.4) to obtain

(3.5) $$e_{OUT} = \left(1+\frac{R_1}{R_2}\right)\cdot e_1 - \frac{R_1}{R_2}\cdot e\left(1+\frac{R_3}{R_4}\right)\cdot e_2 .$$

Note that when $R_1 \cdot R_3 = R_2 \cdot R_4$ this is a differential amplifier with theoretically zero common-mode gain; the output is a function of $\left(e_1 - e_2\right)$ but not $\left(e_1 + e_2\right)$.

Problem 4 (20%)

Refer to the MOSFET signal model shown in Figure 6. For an input signal e_{IN} applied at the gate ($v_{Gate} = v_{IN}$),

- Find the Thévenin equivalent circuit between the output marked v_{Source} and ground.
- Find the Thévenin equivalent circuit between the output marked v_{Drain} and ground.

The solutions will be algebraic equations involving the transconductance g and the resistances R_{Bias}, R_S, and R_D.

HINT: Write Kirchhoff's current law for the current node at the source terminal and use the node voltage notation. This will solve the circuit. Then, find the short circuit currents; this is simpler than the virtual source technique.

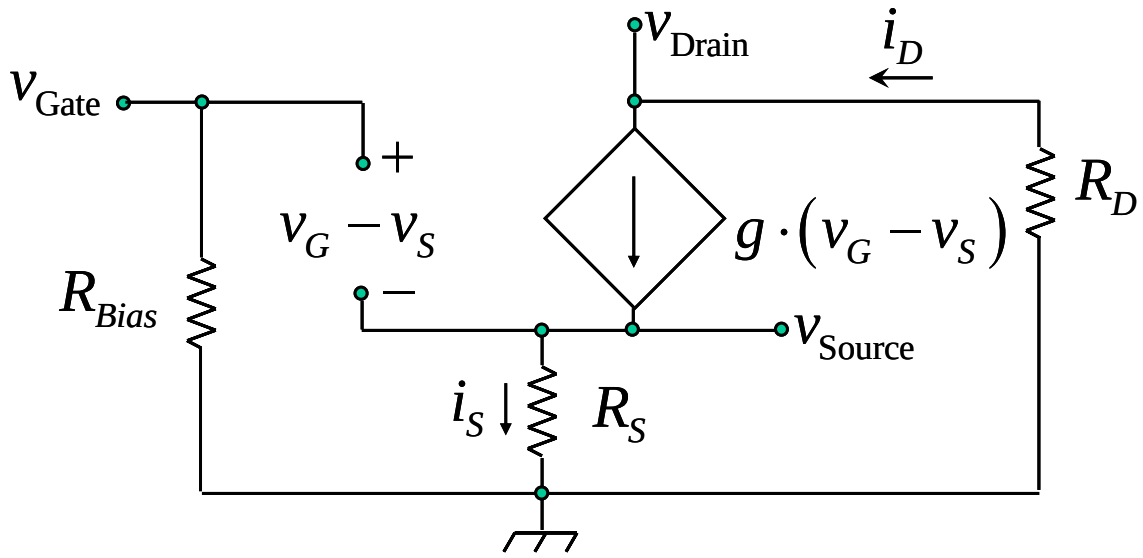

Figure 6. MOSFET Signal Model.

Solution

Since the gate current is zero, the current out of the MOSFET source is the same as the current into the drain, and Kirchhoff's current law simply re-states this. Writing Kirchhoff's current law for the node at the MOSFET source is, in terms of the node voltage v_{Source},

(4.1) $$i_S = \frac{v_S}{R_S} = g \cdot (v_G - v_S) = i_D$$

from which we can find the source voltage v_S

(4.2) $$v_S = \frac{g \cdot R_S}{1 + g \cdot R_S} \cdot v_G$$

which is the open circuit voltage at the MOSFET source terminal. The source current is

(4.3) $$i_S = \frac{v_S}{R_S} = \frac{g}{1 + g \cdot R_S} \cdot v_g \, .$$

We can find the short circuit current as i_S for zero source resistance, i.e. take R_S as zero in (4.3):

(4.4) $$i_{S,SC} = g \cdot v_G \, .$$

The Thévenin equivalent resistance is the open circuit voltage divided by the short circuit current, or

(4.5) $$RS_{TH} = \frac{v_S}{i_{S,SC}} = \frac{R_S}{1 + g \cdot R_S} \, .$$

The current into the drain terminal of the MOSFET is the same as the current out of the source terminal as given by (4.3) and we find the voltage at the drain terminal from Ohm's law as

(4.6) $$v_D = -i_D \cdot R_D = -i_S \cdot R_D = -\frac{g \cdot R_D}{1 + g \cdot R_S} \cdot v_G$$

which is the open circuit voltage at the drain terminal. The short circuit current is simply the negative of the source current as given by (4.3) because the drain current is not a function of R_D, and the Thévenin equivalent resistance at the drain terminal is

(4.7) $$RD_{Th} = \frac{v_D}{-i_D} = R_D \, .$$

This can be seen by the principle of superposition and the test source method because, when the gate voltage v_G is taken as zero the current in the controlled source is zero and the impedance seen at the drain terminal is simply R_E.

Problem 5 (20%)

This is a BJT biasing problem. Refer to Figure 7 for the circuit and Figure 8 for the biasing model. The problem is to design a BJT amplifier that meets these requirements:

- Given an NPN transistor with a minimum current gain β_{MIN} of 150, and a base-emitter voltage drop V_f of 0.7 Volts,
- A collector supply voltage V_{CC} of 15 Volts,
- We require an output impedance of 10 kOhms,
- We require a gain of 25,
- We require that the collector voltage be approximately $V_{CC}/2$ or 7.5 Volts when there is no signal present, and
- We require here that you define the Thévenin equivalent circuit for the bias circuit shown inside the dotted lines in Figure 8, not the voltage divider resistors.

Give the values of the resistances in Figure 8, the voltages at the transistor terminals, and the transistor base and collector currents.

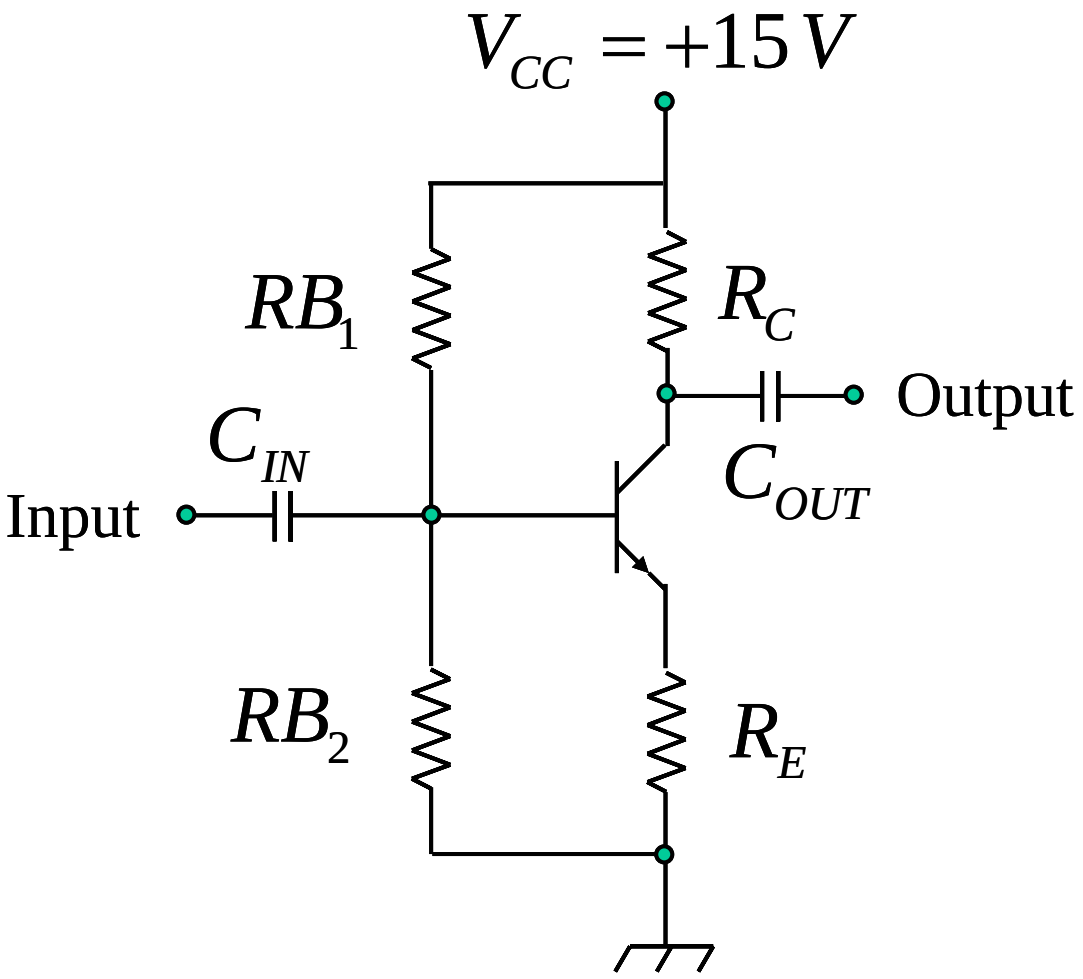

Figure 7. BJT Inverting Amplifier Biasing Circuit.

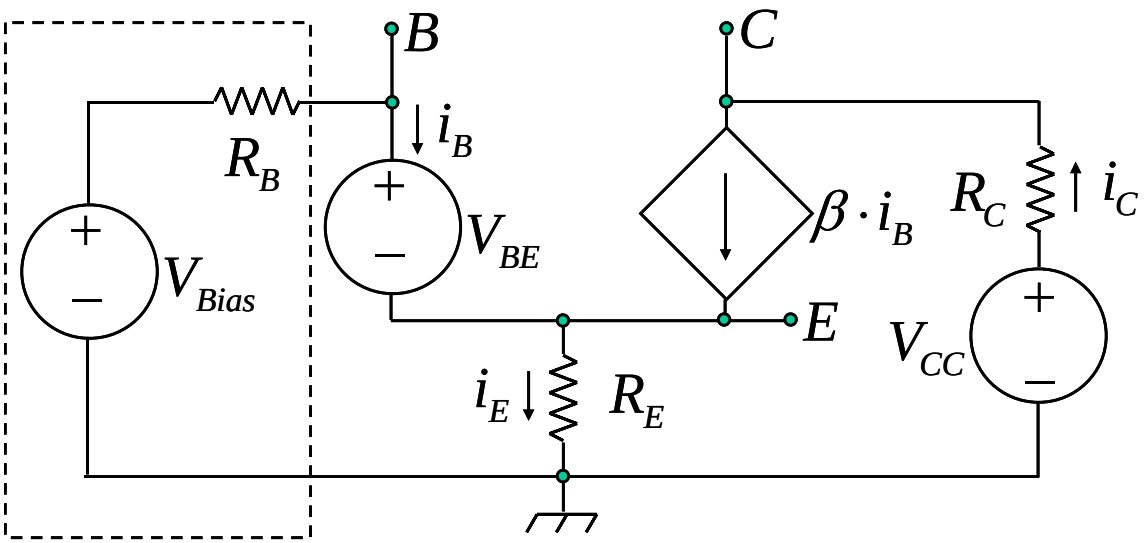

Figure 8. BJT Inverting Amplifier Biasing Model.

Note that the Thévenin equivalent circuit for the bias components RB_1, RB_2 and V_{CC} is inside the dotted box in the bias model shown in Figure 8. Find the maximum allowable value of R_B that will allow robust operation of the circuit for current gain at or above the minimum β_{MIN} of 150 as given in the problem statement.

Solution

Since the AC or incremental small signal gain for the BJT is, for the purposes of this problem, the same as the DC current gain, the signal model can bet taken from the bias model, Figure 8 by dropping the DC voltages. The output impedance at the collector terminal of the BJT can be seen from this to be simply R_C; this can be seen by taking the base voltage as zero and using the test source method. Thus, the maximum collector resistance R_C that will provide an inverting amplifier with the required impedance of 10,000 Ohms is 10,000 Ohms,

(5.1) $$R_C = 10,000\,\Omega .$$

We know from our signal model and the fact that we have a moderate to high current gain β that the gain G is approximately $-R_C/R_E$, so the proper value of the emitter resistor R_E is

(5.2) $$R_E = \frac{R_C}{G} = \frac{10000\,\Omega}{25} = 400\,\Omega .$$

We require that the collector voltage be approximately 7.5 Volts, so the collector resistor R_C must have a voltage drop of $(15-7.5)$ Volts or again 7.5 Volts, so the collector current is to be set at

(5.3) $$i_C = \frac{7.5\,V}{10000\,\Omega} = 0.75\,mA.$$

The emitter voltage is about $1/G$ times this or

(5.4) $$v_E = i_E \cdot R_E \approx i_C \cdot R_E = 0.3\,Volts.$$

Since we are given a base to emitter voltage drop V_f in the problem statement of 0.7 Volts, we now have the base voltage v_B as

(5.5) $$v_B = v_E + V_V = 0.3\,Volts + 0.7\,Volts = 1\,Volt.$$

We require that the Thévenin equivalent resistance of the bias source be small enough for robust operation as an inverting amplifier. This means that we must provide a voltage V_{Bias} that is approximately the base voltage v_B and a resistance that is much smaller than the Thévenin equivalent resistance seen at the base terminal,

(5.6) $$RB_{Th} = (1+\beta)\cdot R_E$$

which we can obtain from the signal model obtained from Figure 8 by dropping the DC voltages and using the test source method to the right of the dotted line. We have a minimum current gain β_{MIN} of 150 from the problem statement, so we have

(5.7) $$\begin{cases} V_{Bias} = 1\,Volt \\ R_B \ll 60,000\,\Omega. \end{cases}$$

I will accept other valid methods of establishing the bias voltage and Thévenin equivalent resistance.