Bipolar Junction Transistor Amplifiers
Biasing, Gain, Input and Output

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Biasing of Bipolar Junction Transistor Amplifiers

1 Introduction

We begin with the concept of a bipolar junction transistor (BJT) in the inverting amplifier configuration, with an emitter resistor and the base bias provided by a voltage divider from the main supply voltage. The goal is to understand and design an amplifier for maximum voltage swing on output, or for small signal with minimum power or lowest noise.

We use one model for our biasing analysis and a separate model for our signal model. Our biasing analysis model is a simple constant voltage drop for the base-emitter junction. The *h-parameter* value of input resistance is used with the signal model but not with the bias model. The *h-parameter* base-collector current gain is used in both the biasing analysis and signal models. The *h-parameter* collector resistance is neglected in both models, as is the collector-base feedback coupling coefficient.

Our biasing analysis begins with the use Kirchhoff's laws[1] to solve the bias model. The load line is presented and we include here the concept of the use of the collector and emitter resistors to limit transistor power dissipation. The bias circuit analysis concludes with the Thévenin equivalent circuits for the three transistor terminals

The signal analysis uses a different model that omits DC voltage sources and includes the base terminal input resistance. Input and output capacitive coupling is also included in the signal model.

We conclude with a section on design of BJT inverting amplifiers. This analysis begins with simplification of the equations developed from the biasing and signal models by looking at the engineering approximations, and the design constraints required to support the accuracy and usefulness of these approximations. Then these approximations are used in a simple step-by-step process of designing a robust BJT amplifier in an inverting configuration.

The emitter follower is supported by the models and analyses prepared for the inverting amplifier. The biasing and design of a robust emitter follower concludes the design section.

2 Simplified Equivalent Circuit

We will consider a bipolar junction transistor (BJT) in an inverting amplifier configuration, which is biased according to the feedback-bias circuit[2] given below as Figure 1.

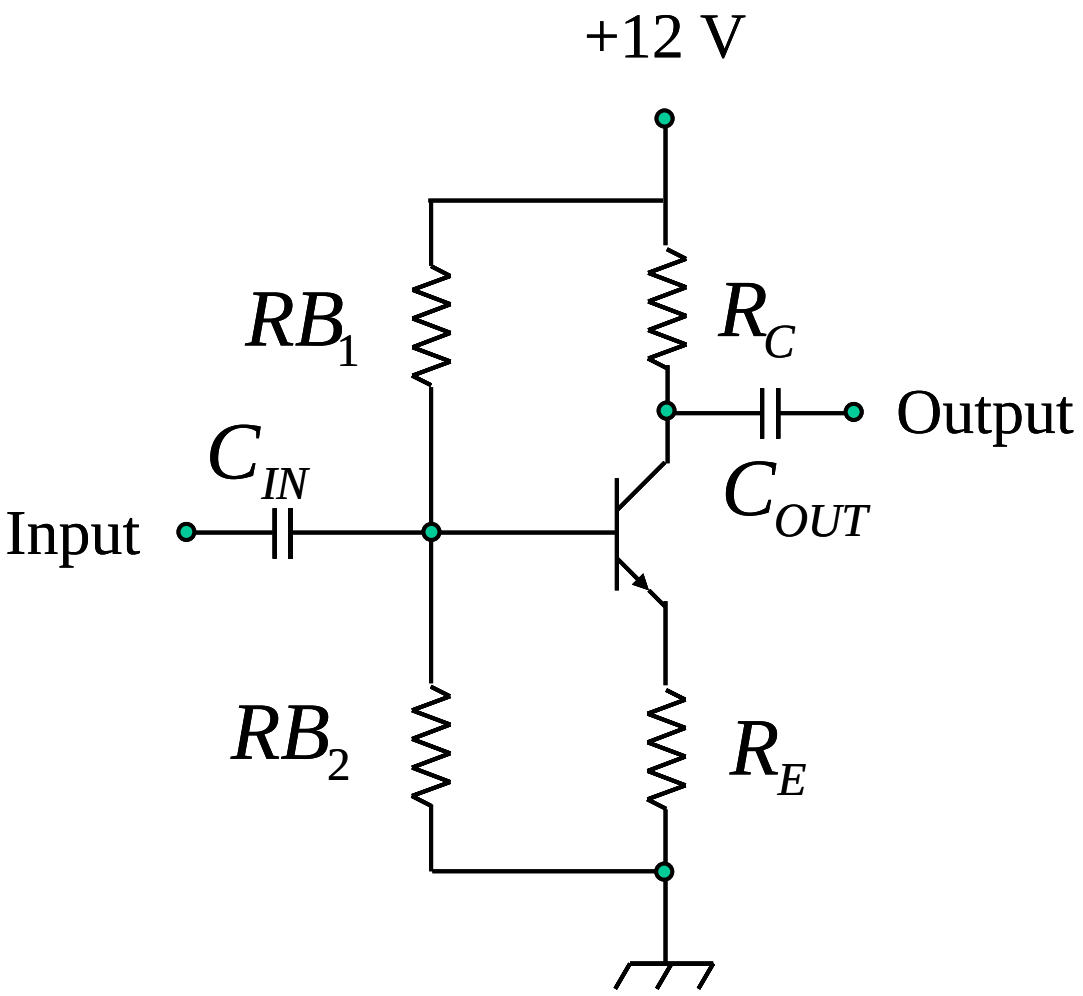

Figure 1. BJT in Inverting Amplifier Circuit with Bias Circuitry.

This is the configuration most often used for BJT amplifiers in either the inverting amplifier or emitter follower configuration. Most analysis that follows is directed to the inverting amplifier but we have a short section on the emitter follower, which is obtained from the circuit of Figure 1 simply by taking the value of the collector load resistor R_C as zero and obtaining the output from the emitter terminal.

The circuit shown in Figure 2 is a simplified model of BJT. The portion of the circuit inside the doted rectangle is a Thévenin equivalent circuit of the biasing circuitry, not the actual biasing circuit. The base, emitter, and collector terminals are denoted by B, E and C respectively. The base-emitter diode junction is modeled by a constant voltage drop, shown in Figure 2 as the source V_{BE}, which for most silicon transistors is about 0.7 Volts.

This is simpler than the *h parameter* model used in SPICE and other detailed models. The intent here is to provide a simple analysis and design method that enables design of

robust BJT inverting amplifiers and emitter followers from data sheet parameters without additional computer models.

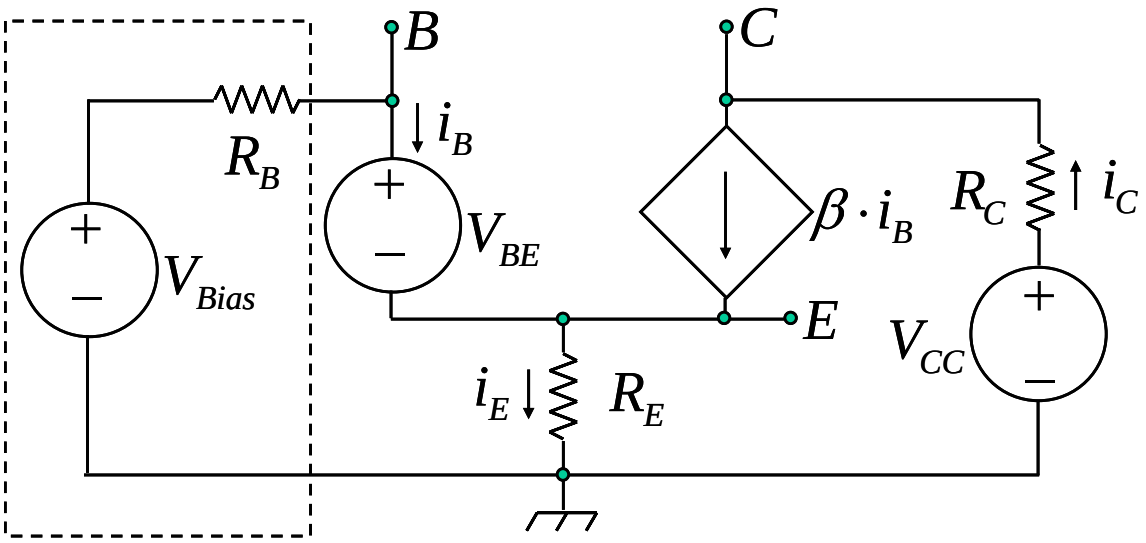

Figure 2. Simple Transistor Model of BJT Inverting Amplifier with Feedback Bias Circuit.

The circuit of Figure 2 is similar to those considered in Example 1.3, pages 10-12, and homework problem 1.65 (a) on page 33. The principal difference is that the transistor model in Figure 2 models the base-emitter junction as a voltage drop rather than a resistance. Note that for most BJTs in normal operation, the base current is on the order of 1 to 100 microamperes, and the dynamic resistance of a diode forward biased with so low a current will not be negligible. As explained in the text, section 3.3.3 page 120, the diode v-i curve is given by

(2.1) $$i_D(v_D) = I_S \cdot \left(\exp\left(\frac{v_D}{\eta \cdot V_T} \right) - 1 \right)$$

where η (the Greek letter eta) is the emission coefficient and is normally between 1 and 2, I_S is the saturation current and is most simply measured as the diode current under reverse bias, v_D is the voltage across the diode, and V_T is the thermal voltage. The thermal voltage the potential equivalent to the thermal energy of an electron and is given by

(2.2) $$V_T = \frac{k \cdot T}{q}.$$

The equivalent series resistance is given by

(2.3) $$\frac{1}{Req} = \frac{\partial i_D}{\partial v_D} = \frac{I_S}{\eta \cdot V_T} \cdot \exp\left(\frac{v_D}{\eta \cdot V_T} \right).$$

For forward biased diodes, we see that

$$Req = \frac{\eta \cdot V_T}{i_D + I_S} \approx \frac{\eta \cdot V_T}{i_D}. \tag{2.4}$$

For a typical silicon base-emitter junction, η is about 1.65, V_T is about 0.025 volts at room temperature, and

$$Req = \frac{4125}{i_D}\,\Omega \text{ (for } i_D \text{ in microamperes)}. \tag{2.5}$$

For a base current of 10 microamperes, the dynamic equivalent resistance of the base-emitter junction will be about $400\,\Omega$. Note that the junction temperature determines V_T and may be as much as 50 C higher than room temperature, and *Req* can be up to 15% higher than that predicted by (2.5). For the purposes of signal and gain analysis, the value of *Req* should be added to the circuit in place with the source V_{EB} and accounted for in the Thévenin equivalent resistance of the bias circuit. We will revisit this when we talk about passing signals through the amplifier.

3 Solving the Bias Circuit

3.1 The Node Voltage Equations

Here we will use Kirchhoff's current law with node voltage notation. The nodes in the circuit of Figure 1 and the model of Figure 2 are the terminals for the base B, emitter E, and collector C of the transistor. Note that since we model the base-emitter diode as a constant voltage source, the base and emitter is a supernode. The node equations are

$$\begin{cases} \text{Emitter, Base} & i_E - i_B - \beta \cdot i_B = 0 \\ \text{Collector} & \beta \cdot i_B - i_C = 0. \end{cases} \tag{3.1}$$

To use the node voltage notation, we need Ohm's law to pose each of the currents in terms of the node voltages:

$$\begin{cases} i_B = \dfrac{V_{Bias} - \left(V_E + V_{BE}\right)}{R_B} \\ i_E = \dfrac{V_E}{R_E} \\ i_C = \dfrac{V_{CC} - V_C}{R_C}. \end{cases} \tag{3.2}$$

Substituting (3.2) into (3.1) gives us the node voltage equations

(3.3)
$$\begin{cases} \text{Emitter, Base} & \dfrac{V_E}{R_E}-(1+\beta)\cdot\dfrac{V_{Bias}-V_{BE}-V_E}{R_B}=0 \\ \text{Collector} & \beta\cdot\dfrac{V_{Bias}-V_{BE}-V_E}{R_B}-\dfrac{V_{CC}-V_C}{R_C}=0 \end{cases}$$

In matrix form these equations are

(3.4)
$$\begin{bmatrix} \dfrac{1}{R_E}+\dfrac{1+\beta}{R_B} & 0 \\ -\dfrac{\beta}{R_B} & \dfrac{1}{R_C} \end{bmatrix}\cdot\begin{bmatrix} V_E \\ V_C \end{bmatrix}=\begin{bmatrix} \dfrac{1+\beta}{R_B}\cdot(V_{Bias}-V_{BE}) \\ \dfrac{V_{CC}}{R_C}-\dfrac{\beta}{R_B}\cdot(V_{Bias}-V_{BE}) \end{bmatrix}$$

Note that the top row has no dependence on the collector voltage V_C. This is because our simplified transistor model puts a controlled current source between the collector terminal and the rest of the circuit, so that the collector voltage does not affect the base and emitter portions of the circuit.

3.2 The Circuit Voltages and Currents

Equation (3.4) has the solution

(3.5)
$$\begin{bmatrix} V_E \\ V_C \end{bmatrix}=\begin{bmatrix} \dfrac{1}{\dfrac{1}{R_E}+\dfrac{1+\beta}{R_B}} & 0 \\ \dfrac{\beta\cdot R_C/R_B}{\dfrac{1}{R_E}+\dfrac{1+\beta}{R_B}} & R_C \end{bmatrix}\cdot\begin{bmatrix} \dfrac{1+\beta}{R_B}\cdot(V_{Bias}-V_{BE}) \\ \dfrac{V_{CC}}{R_C}-\dfrac{\beta}{R_B}\cdot(V_{Bias}-V_{BE}) \end{bmatrix}$$

or, multiplying through the matrix and vector on the right hand side and simplifying to obtain equations for further use,

(3.6)
$$\begin{cases} V_E=\dfrac{(1+\beta)\cdot R_E}{R_B+(1+\beta)\cdot R_E}\cdot(V_{Bias}-V_{BE}) \\ V_C=V_{CC}-\dfrac{\beta\cdot R_C}{R_B+(1+\beta)\cdot R_E}\cdot(V_{Bias}-V_{BE}). \end{cases}$$

An important equation in working with the load line and circuit design is the collector to emitter voltage,

(3.7)
$$V_{CE}=V_C-V_E=V_{CC}-\frac{\beta\cdot R_C+(1+\beta)\cdot R_E}{R_B+(1+\beta)\cdot R_E}\cdot(V_{Bias}-V_{BE}).$$

With (3.6) and (3.2) we have the base current, and with (3.1) the collector and emitter currents as

$$\text{(3.8)} \qquad \begin{cases} i_B = \dfrac{V_{Bias} - V_{BE}}{R_B + (1+\beta)\cdot R_E} \\ i_C = \beta \cdot i_B \\ i_E = (1+\beta)\cdot i_B \,. \end{cases}$$

3.3 Thévenin and Norton Equivalent Circuits for the Base, Emitter and Collector

3.3.1 The Thévenin Equivalent Circuit for the Collector

The collector circuit of Figure 2 presents us with a Thévenin equivalent circuit with parameters

$$\text{(3.9)} \qquad \begin{cases} VC_{OC} = V_C = V_{CC} - \dfrac{\beta \cdot R_C \cdot (V_{Bias} - V_{BE})}{R_B + (1+\beta)\cdot R_E} \\ IC_{SC} = \dfrac{V_{CC}}{R_C} - i_C = \dfrac{V_{CC}}{R_C} - \dfrac{\beta \cdot (V_{Bias} - V_{BE})}{R_B + (1+\beta)\cdot R_E} \\ RC_{EQ} = \dfrac{VC_{OC}}{IC_{OC}} = R_C \,. \end{cases}$$

Note that the short circuit current is idealized and taken from the model of Figure 2. For a practical circuit designed for maximum voltage swing, the operating point will be defined so that the collector voltage V_C will be about $V_{CC}/2$.

3.3.2 The Thévenin Equivalent Circuit for the Emitter

The circuit of Figure 1 can be used as an emitter follower by taking the value of the collector resistor R_C as zero. Thus we have an interest in looking at the emitter terminal as an alternate output of the circuit, where the amplifier is configured as an emitter follower. We can look at the Thévenin equivalent by evaluating the open circuit voltage and short circuit current using the model of Figure 2,

(3.10)
$$\begin{cases} VE_{OC} = V_E = \dfrac{(1+\beta)\cdot R_E}{R_B + (1+\beta)\cdot R_E}\cdot (V_{Bias} - V_{BE}) \\ IE_{SC} = (1+\beta)\cdot \dfrac{V_{Bias} - V_{BE}}{R_B} \\ RC_{TH} = \dfrac{VE_{OC}}{IE_{SC}} = \dfrac{R_B \cdot R_E}{R_B + (1+\beta)\cdot R_E} = \dfrac{1}{\dfrac{1}{R_E} + \dfrac{1+\beta}{R_B}} \end{cases}$$

Note that the Thévenin equivalent resistance for the emitter follower is the parallel combination of the value of the emitter resistor and $1/(1+\beta)$ times the base resistance, a value that appears in (3.4) and (3.5).

3.3.3 The Thévenin Equivalent Circuit for the Base

The open circuit voltage for the base is V_B can be seen from Figure 2 to be the emitter voltage V_E as given by (3.6), plus the base-emitter voltage V_{BE},

(3.11)
$$\begin{aligned} VB_{OC} = V_E + V_{BE} &= \frac{(1+\beta)\cdot R_E \cdot (V_{Bias} - V_{BE})}{R_B + (1+\beta)\cdot R_E} + V_{BE} \\ &= \frac{(1+\beta)\cdot R_E \cdot V_{Bias} + R_B \cdot V_{BE}}{R_B + (1+\beta)\cdot R_E}. \end{aligned}$$

The short circuit current requires a little finesse to use existing results without a new circuit solution, but can be discerned from (3.8) by taking V_{Bias} as 0 Volts and R_B as zero in that equation to find i_B, then subtracting this current from V_{Bias}/R_B,

(3.12)
$$IB_{SC} = \frac{V_{Bias}}{R_B} + \frac{V_{BE}}{(1+\beta)\cdot R_E}.$$

The Thévenin resistance is the ratio,

(3.13)
$$RB_{EQ} = \frac{(1+\beta)\cdot R_B \cdot R_E}{R_B + (1+\beta)\cdot R_E} = \frac{1}{\dfrac{1}{(1+\beta)\cdot R_E} + \dfrac{1}{R_B}}.$$

Interestingly enough, this is $(1+\beta)$ times the parallel combination of the emitter resistance and the base resistance divided by $(1+\beta)$, the Thévenin resistance at the emitter.

4 The Load Line

4.1 Drawing the Load Line

The load line is a straight line on a set of transistor collector-emitter v-i curves that reflects the Thévenin equivalent circuit made up of the supply voltage V_{CC} and the collector and emitter circuit resistance $\left(R_C + R_E\right)$. Figure 3 shows a load line on a typical NPN BJT transistor. The load line intercepts the voltage axis at V_{CC} and the current axis at $V_{CC}/\left(R_C + R_E\right)$. The transistor can operate as a linear amplifier only when the operating point is on the load line in a region between saturation and cutoff.

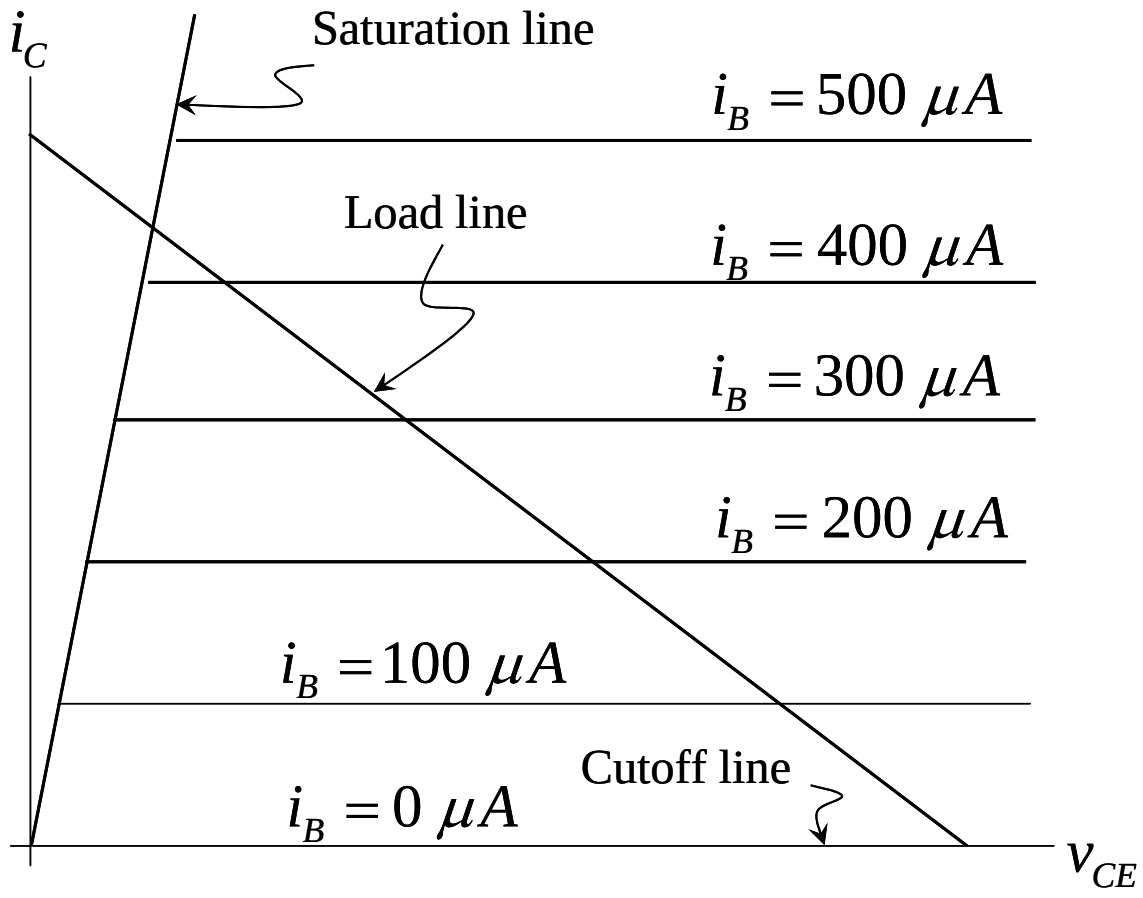

Figure 3. Idealized v-i Curve and Load Line for a BJT.

4.2 Controlling the Power Dissipated in the Transistor

An important addition to the load line is a curve of allowable power dissipation for the transistor. This is a hyperbola on the v-i curve with asymptotes of the v and i axes. The region between this curve and the axes represents the allowable operation region of the

transistor, where the power dissipated does not exceed the maximum allowed. The equation for the allowed region is

(4.1) $$V_{CE} \cdot i_C < P_{MAX} .$$

The load line can cross the hyperbola and part of it may be outside the allowed region. But, the zero-signal operating point must be inside the allowed region.

The value of the collector resistor R_C plus that of the emitter resistor R_E can be defined to limit the maximum possible power available to the transistor. We know by maximum power transfer principles that this power is

(4.2) $$PMAX_{Transistor} = \frac{V_{CC}^2}{4 \cdot (R_C + R_E)}$$

so we can ensure that the maximum power dissipated by a transistor will never exceed a specified maximum by limiting R_C according to

(4.3) $$R_C + R_E \geq \frac{V_{CC}^2}{4 \cdot P_{MAX}} .$$

5 Solving the Signal Model

5.1 The Signal Equivalent Circuit

The signal equivalent circuit is shown in Figure 4. Here we must consider the dynamic base-emitter resistance as given by (2.4); we denote this resistance as R_{BB} in the figure. There are three independent voltage nodes in this circuit because the base and emitter nodes are not a supernode as with the bias model.

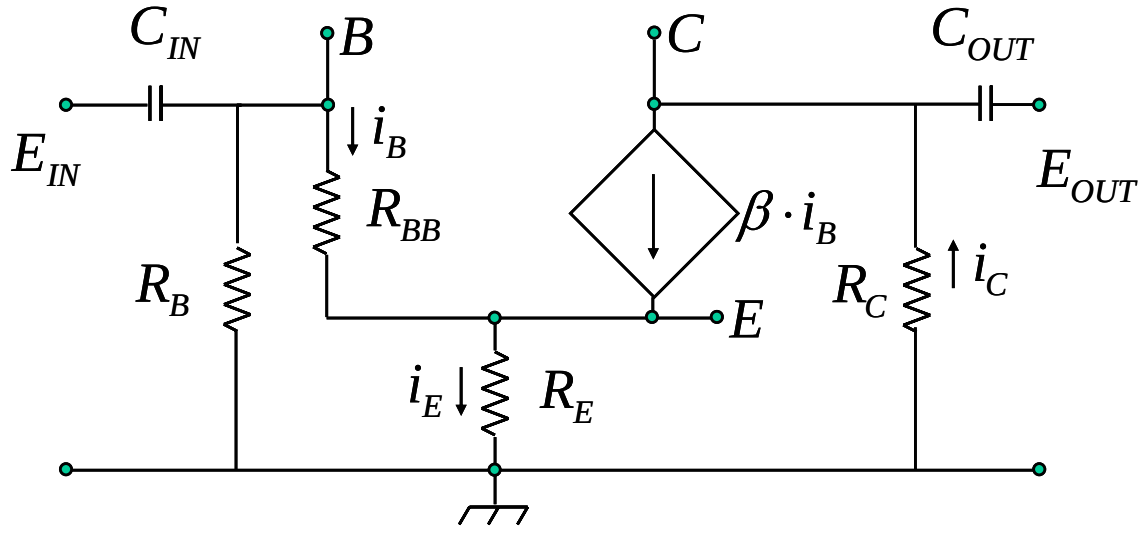

Figure 4. Signal Model of Circuit of Figure 1

5.2 The Equivalent Base Resistance

The base to emitter resistance R_{BB} has two principal components. The equivalent dynamic impedance of the forward-biased base-emitter diode is

$$R_{BB} = R_{Ohmic} + \frac{\eta \cdot V_{JT}}{i_B + I_S} \approx R_{Ohmic} + \frac{\eta \cdot V_{JT}}{i_B} \tag{5.1}$$

where R_{Ohmic} is the actual resistance of components of the transistor, and V_{JT} is the thermal voltage corresponding to the junction temperature T_J,

$$V_{JT} = \frac{k \cdot T_J}{q} \tag{5.2}$$

where k is Boltzman's constant and q is the electron charge in Coulombs,

$$\begin{cases} k = 1.380662 \cdot 10^{-23} \ \dfrac{J}{K} \\ q = 1.6021892 \cdot 10^{-19} \ C \, . \end{cases} \tag{5.3}$$

The junction temperature exceeds the ambient temperature due to the heat dissipated by the power used by the transistor. The temperature rise is

$$T_{RISE} = P_{Trans} \cdot R_{\theta JA} \tag{5.4}$$

where $R_{\theta JA}$ is the thermal resistance from the junction to ambient. For the 2N3904 in TO-92 case,

$$R_{\theta JA} = 200 \ \frac{^\circ C}{W} \text{ (2N3904 in TO-92 case)} \tag{5.5}$$

which for 50 milliwatts will give us a 10 degrees Centigrade temperature rise. The typical dynamic input resistance for the 2N3904 from the Fairchild Semiconductor data sheet[3] is shown in Figure 5.

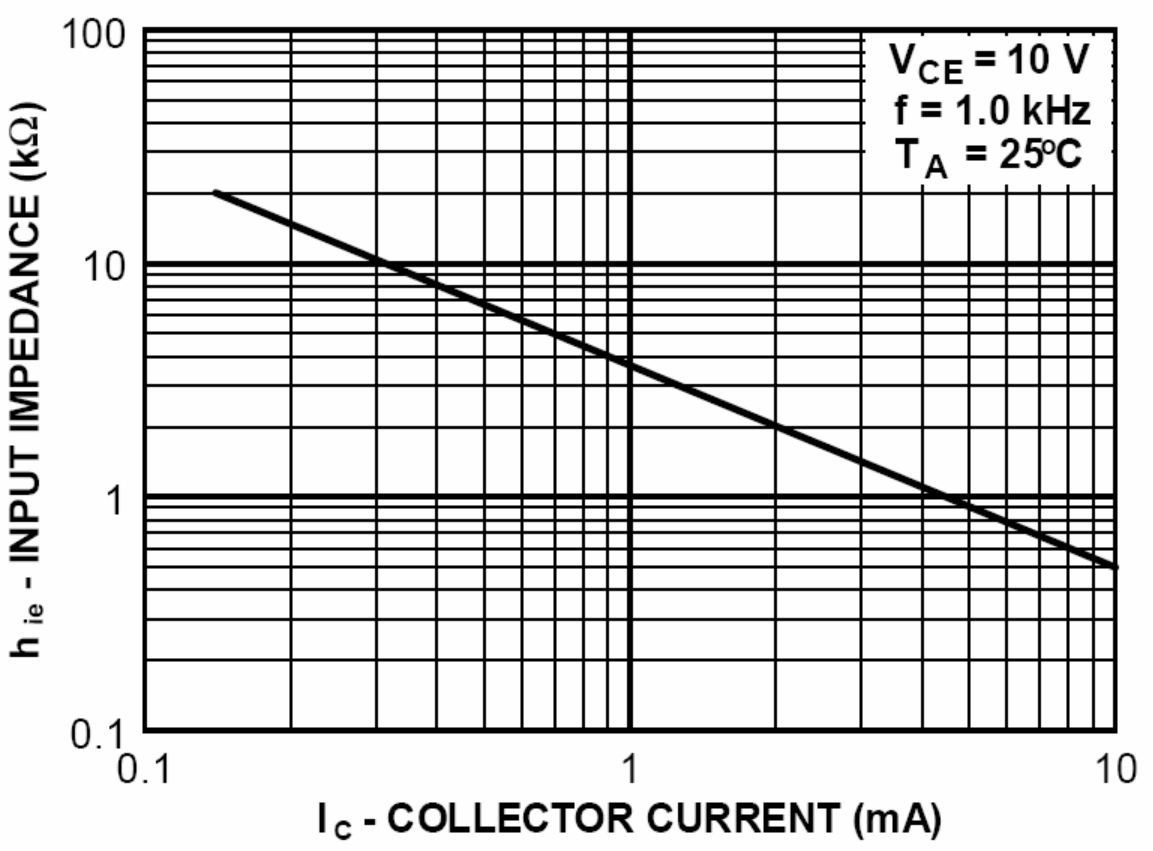

Figure 5. Input Impedance of 2N3904 from Fairchild Data Sheet.

5.3 The Node Voltage Equations

In the signal model, we will use the symbol E for voltages to distinguish them from bias and power voltages. Note that we have capacitive coupled inputs and outputs. We use complex impedance to analyze these circuits, which means that we are considering steady state solutions with sine wave inputs. The capacitive impedances are denoted by

$$\begin{cases} Z_{IN} = \dfrac{1}{j \cdot \omega \cdot C_{IN}} \\ Z_{OUT} = \dfrac{1}{j \cdot \omega \cdot C_{OUT}} \end{cases} \tag{5.6}$$

and we treat the input capacitance with circuit theory. The output here is not represented as a load, so the output voltage is the same as the collector voltage because there is no current through Z_{OUT}. We support the addition of an output load by the Thévenin equivalent for the output circuit that includes Z_{OUT}.

We have a controlled source, so we will explicitly write the equation for the controlling current i_B,

$$i_B = \frac{E_B - E_E}{R_{BB}}$$

For the base node, the currents out of the node are:

$$\frac{E_B - E_{IN}}{Z_{IN}} + \frac{E_B}{R_B} + \frac{E_B - E_E}{R_{BB}} = 0 . \tag{5.7}$$

For the emitter node:

$$-\frac{E_B - E_E}{R_{BB}} + \frac{E_E}{R_E} - \beta \cdot \frac{E_B - E_E}{R_{BB}} = 0 \tag{5.8}$$

For the collector node:

$$\beta \cdot \frac{E_B - E_E}{R_{BB}} + \frac{E_C}{R_C} = 0 . \tag{5.9}$$

These equations, arranged in matrix form, become

$$\begin{bmatrix} \frac{1}{Z_{IN}} + \frac{1}{R_B} + \frac{1}{R_{BB}} & -\frac{1}{R_{BB}} & 0 \\ -\frac{1+\beta}{R_{BB}} & \frac{1+\beta}{R_{BB}} + \frac{1}{R_E} & 0 \\ \frac{\beta}{R_{BB}} & -\frac{\beta}{R_{BB}} & \frac{1}{R_C} \end{bmatrix} \cdot \begin{bmatrix} E_B \\ E_E \\ E_C \end{bmatrix} = \begin{bmatrix} \frac{E_{IN}}{Z_{IN}} \\ 0 \\ 0 \end{bmatrix} . \tag{5.10}$$

5.4 The Circuit Voltages and Currents

From (5.10) we have the base voltage,

$$E_B = \frac{R_B \cdot \left((1+\beta) \cdot R_E + R_{BB} \right)}{R_B \cdot \left((1+\beta) \cdot R_E + R_{BB} \right) + Z_{IN} \cdot \left((1+\beta) \cdot R_E + R_{BB} + R_B \right)} \cdot E_{IN} \tag{5.11}$$

the emitter voltage,

$$E_E = \frac{(1+\beta) \cdot R_E \cdot R_B}{R_B \cdot \left((1+\beta) \cdot R_E + R_{BB} \right) + Z_{IN} \cdot \left((1+\beta) \cdot R_E + R_{BB} + R_B \right)} \cdot E_{IN} \tag{5.12}$$

and the collector voltage,

$$E_C = -\frac{\beta \cdot R_B \cdot R_C}{R_B \cdot \left((1+\beta) \cdot R_E + R_{BB} \right) + Z_{IN} \cdot \left((1+\beta) \cdot R_E + R_{BB} + R_B \right)} \cdot E_{IN} . \tag{5.13}$$

The currents are found by using (5.11), (5.12), (5.13) and Ohm's law. The base current is

$$i_B = \frac{E_B - E_E}{R_{BB}} = \frac{R_B \cdot E_{IN}}{R_B \cdot \left((1+\beta) \cdot R_E + R_{BB} \right) + Z_{IN} \cdot \left((1+\beta) \cdot R_E + R_{BB} + R_B \right)} , \tag{5.14}$$

the emitter current is

$$i_E = \frac{E_E}{R_E} = \frac{(1+\beta) \cdot R_B \cdot E_{IN}}{R_B \cdot \left((1+\beta) \cdot R_E + R_{BB} \right) + Z_{IN} \cdot \left((1+\beta) \cdot R_E + R_{BB} + R_B \right)} \tag{5.15}$$

and the collector current is

$$i_C = \beta \cdot i_B = \frac{\beta \cdot R_B \cdot E_{IN}}{R_B \cdot \left((1+\beta) \cdot R_E + R_{BB} \right) + Z_{IN} \cdot \left((1+\beta) \cdot R_E + R_{BB} + R_B \right)} . \tag{5.16}$$

5.5 Thévenin Equivalent Circuits for the Transistor Terminals

The open circuit voltages are given by (5.11), (5.12) and (5.13). For the base circuit we use the virtual source technique, and treat E_{IN} as the virtual source. The current produced by E_{IN} into the input terminal is

(5.17) $$iB_{SC} = i_B + \frac{E_B}{R_B} = \frac{\left(1+\beta\right)\cdot R_E + R_{BB} + R_B}{R_B \cdot \left(\left(1+\beta\right)\cdot R_E + R_{BB}\right) + Z_{IN} \cdot \left(\left(1+\beta\right)\cdot R_E + R_{BB} + R_B\right)} \cdot E_{IN} .$$

The short circuit current for the emitter is given by (5.15) with R_E taken as zero,

(5.18) $$iE_{SC} = \frac{\left(1+\beta\right)\cdot R_B \cdot E_{IN}}{R_B \cdot R_{BB} + Z_{IN} \cdot \left(R_{BB} + R_B\right)}$$

and the short circuit collector current is given by (5.16).

The Thévenin equivalent resistances are the ratios of the open circuit voltages and the short circuit currents. The Thévenin equivalent resistance for the base is

(5.19) $$ZB_{EQ} = \frac{R_B \cdot \left(\left(1+\beta\right)\cdot R_E + R_{BB}\right)}{\left(1+\beta\right)\cdot R_E + R_{BB} + R_B}$$

which is the resistance of R_B and $\left(\left(1+\beta\right)\cdot R_E + R_{BB}\right)$ in parallel, the Thévenin equivalent resistance for the emitter is

(5.20) $$ZE_{EQ} = \frac{R_E \cdot \left(R_B \cdot R_{BB} + Z_{IN} \cdot \left(R_{BB} + R_B\right)\right)}{R_B \cdot \left(\left(1+\beta\right)\cdot R_E + R_{BB}\right) + Z_{IN} \cdot \left(\left(1+\beta\right)\cdot R_E + R_{BB} + R_B\right)}$$

and the Thévenin equivalent resistance for the collector is

(5.21) $$ZC_{EQ} = R_C .$$

5.6 Thévenin Equivalent Circuits for the Input and Output Terminals

The Thévenin equivalent impedance for the input terminal is the sum of the impedance o of the input capacitor and the Thévenin equivalent resistance of the base circuit,

(5.22) $$ZIN_{EQ} = Z_{IN} + ZB_{EQ}$$

where ZB_{EQ} is given by (5.19). The Thévenin equivalent impedance for the output terminal is the sum of the value of the collector resistor and the output capacitor,

(5.23) $$ZOUT_{EQ} = R_C + Z_{OUT} .$$

5.7 Amplifier Gain

5.7.1 Voltage Gain of the Inverting Amplifier

The inverting amplifier voltage gain is the ratio of output voltage to input voltage. Neglecting input impedance (i.e. assuming that input impedance is low relative to ZIN_{EQ}) and output impedance (i.e. assuming that output impedance is high relative to $ZOUT_{EQ}$), this ratio is available from (5.13) as

(5.24) $$G_{INV} = -\frac{\beta \cdot R_B \cdot R_C}{R_B \cdot \left((1+\beta)\cdot R_E + R_{BB}\right) + Z_{IN} \cdot \left((1+\beta)\cdot R_E + R_{BB} + R_B\right)}.$$

If the output of an inverting amplifier subjected to a load Z_L that is not large with regard to R_C is desired, the Thévenin equivalent circuit of the collector terminal provides a simple equation,

(5.25) $$GL_{INV} = \frac{\frac{Z_L}{Z_L + R_C}\cdot E_C}{E_{IN}} = \frac{Z_L}{Z_L + R_C}\cdot G_{INV}.$$

5.7.2 Voltage Gain of the Emitter Follower

The emitter follower voltage gain is the ratio of output voltage to input voltage. Neglecting input impedance (i.e. assuming that input impedance is low relative to ZIN_{EQ}) and output impedance (i.e. assuming that output impedance is high relative to that of an output coupling capacitor $ZOUT_{EQ}$), this ratio is available from (5.12) as

(5.26) $$G_{EF} = \frac{(1+\beta)\cdot R_E \cdot R_B}{R_B \cdot \left((1+\beta)\cdot R_E + R_{BB}\right) + Z_{IN} \cdot \left((1+\beta)\cdot R_E + R_{BB} + R_B\right)}.$$

In the event that the output of an emitter follower subjected to a load Z_L that is not large with regard to the very low impedance ZE_{EQ} given by (5.20) is desired, the Thévenin equivalent circuit of the output provides a simple equation,

(5.27) $$GL_{EF} = \frac{Z_L}{Z_L + Z_{OUT} + ZE_{EQ}}$$

where ZE_{EQ} is the Thévenin equivalent resistance seen at the emitter as given by (5.20).

6 Designing for Robustness with Variations in Transistor Current Gain

6.1 Simple Engineering Approximations of the Bias Circuit

The principal production variation between transistors of a given part number is the current gain β of the transistor. We have noted that the operating point of the transistor must be between saturation and cutoff, and that maximum output voltage swing is achieved when the operation point is halfway between the minimum collector voltage at which the transistor enters the saturation region, and cutoff, when the collector voltage reaches V_{CC}.

With the amplifier circuit configuration of Figure 1 and the circuit analysis based on the simple transistor model in that circuit given in Figure 2, we can use the equations for the circuit parameters developed and given in Section 3 above.

An engineering approach to using the equations of Section 3 is to rewrite them for very large β and examine the conditions for these equations being accurate. The voltages for high β are, by taking the limit as β increases without bound in (3.6) and (3.7), are

$$\begin{cases} VE_{\infty} = V_{Bias} - V_{BE} \\ VC_{\infty} = V_{CC} - \dfrac{R_C}{R_E} \cdot \left(V_{Bias} - V_{BE} \right) \\ VCE_{\infty} = V_{CC} - \left(1 + \dfrac{R_C}{R_E} \right) \cdot \left(V_{Bias} - V_{BE} \right) \end{cases} \tag{6.1}$$

and, from (3.8) the limiting currents as β increases without bound are

$$\begin{cases} iB_{\infty} \approx \dfrac{V_{Bias} - V_{BE}}{\beta \cdot R_E} \to 0 \\ iC_{\infty} = iE_{\infty} = \dfrac{V_{Bias} - V_{BE}}{R_E} . \end{cases} \tag{6.2}$$

Examining (3.6), (3.7), and (3.8), the condition for the accuracy of these equations is

$$R_E \gg \frac{R_B}{\beta} . \tag{6.3}$$

Thus we see the importance of the emitter resistor R_E, and we make this relationship relating it and the base resistor R_E, equation (6.3), a design constraint.

6.2 Simple Engineering Approximations of the Signal Circuit

We can use very simple equations for the solutions for the signal circuit if we take advantage of conventional design practices in the values of the impedances. The first example is that the input and output capacitors will have low impedances relative to those seen at the transistor terminals for frequencies at which the amplifier is designed to operate,

$$\left| Z_{IN} \right| \ll R_B \tag{6.4}$$

and

$$\left| Z_{OUT} \right| \ll R_C . \tag{6.5}$$

We need to add one design constraint to ensure that the emitter resistor has the desired stabilizing effect on the behavior of the transistor in the design,

$$R_E \gg \frac{R_{BB}}{\beta} \tag{6.6}$$

which should be combined with (6.3) as a design constraint. With these in hand and the assumption that $\beta \gg 1$, we have immediately a simplified circuit solution,

$$\begin{cases} E_B \approx E_E \approx E_{IN} \\ E_C \approx -\dfrac{R_C}{R_E} \cdot E_{IN} \\ i_B \approx \dfrac{E_{IN}}{\beta \cdot R_E} \\ i_E \approx i_C \approx \dfrac{E_{IN}}{R_E} \end{cases} \tag{6.7}$$

and the Thévenin equivalent resistances,

$$\begin{cases} ZB_{EQ} \approx (1+\beta) \cdot R_E \\ ZE_{EQ} \approx \dfrac{R_{BB}}{\beta} \end{cases} \tag{6.8}$$

and the gains,

$$\begin{cases} G_{INV} \approx -\dfrac{R_C}{R_E} \\ G_{EF} \approx 1. \end{cases} \tag{6.9}$$

6.3 Using Engineering Approximations to Block Out a Design

We see that the base current is very low for large β and that VB_∞ is equal to V_{Bias}. Since V_{Bias} and R_B are determined by the designer as the Thévenin equivalent of the bias circuit voltage divider, we can use V_{Bias} to determine V_B and thus V_E, and sine V_E and R_E determine the base and collector current, we determine the collector voltage by setting R_C to give us the desired voltage drop to achieve our operating point.

Amplifier gain to signals is an important design consideration. We note the inverting amplifier gain given by (6.9) and use this to control the gain so that the circuit behavior is known from the signal point of view as well as the bias point of view.

The process can be set up as a sequential set of steps:

1. Determine the specified circuit gain and use (6.9) to set this gain.
2. Determine the maximum power allowable and use (4.3) to establish a lower bound $(R_C + R_E)$, or, if maximum power is not a consideration in your design, use the specified maximum impedance at the output to set a value for R_C. Thus gives us approximate values for R_C and R_E:

$$R_C + R_E \geq \frac{V_{CC}^2}{4 \cdot P_{MAX}} \tag{6.10}$$

and

(6.11)
$$\begin{cases} R_C = \dfrac{|G_{Inv}|}{1+|G_{INV}|}\cdot\left(R_E + R_C\right) \\ R_E = \dfrac{1}{1+|G_{INV}|}\cdot\left(R_E + R_C\right). \\ R_E = \dfrac{R_C}{|G_{INV}|} \end{cases}$$

3. Select standard values for R_C and R_E that meet the condition set by (6.10) and that obtain the gain ratio as expressed by (6.9) or (6.11) as closely as possible.
4. Select the collector voltage V_C to obtain the operating point desired. For maximum voltage swing, the collector voltage should be about $V_{CC}/2$ or slightly higher to avoid saturation at the negative peaks of the output waveform. For minimum power or best noise figure, the operating point should be as near cutoff as the output voltage swing will comfortably allow. Define the collector current i_C, and thus the emitter current i_E from Ohm's law,

(6.12)
$$i_C = i_E = \frac{V_{CC} - V_C}{R_C}.$$

5. Again using Ohm's law, find the emitter voltage V_E, and thus the base voltage V_B, from the emitter current i_E and the emitter resistor R_E,

(6.13)
$$\begin{cases} V_E = i_E \cdot R_E \\ V_B = V_E + V_{BE}. \end{cases}$$

6. Set the bias voltage to the base voltage, and find the values of the biasing resistors RB_1 and RB_2 in Figure 1 that meet the condition on R_B as given by (6.3). Noting from Figure 1 and Figure 2 that R_B is the parallel combination of RB_1 and RB_2, and that V_{Bias} is the result of a voltage divider of RB_1 and RB_2 driven by V_{CC}, we select any convenient value of R_B that satisfies (6.3) and find RB_1 and RB_2 from

(6.14)
$$\begin{cases} R_B = 1\Big/\left(\dfrac{1}{RB_1} + \dfrac{1}{RB_2}\right) \ll \beta \cdot R_E \\ RB_1 = \dfrac{V_{CC}}{V_{Bias}} \cdot R_B \\ RB_2 = \dfrac{V_{CC}}{V_{CC} - V_{Bias}} \cdot R_B. \end{cases}$$

7. Find standard values for RB_1 and RB_2 that satisfy (6.14).

At this point, your design is complete. Breadboard your design and check V_C and the gain to make sure that the operating point and gain are as designed. If necessary, adjust RB_2 to compensate for the actual value of V_{BE} for the transistor in use.

7 Conclusions

The use of BJT transistors in inverting amplifiers is supported by the simple robust circuit shown in Figure 1. The design is similar to that of an inverting amplifier in an op-amp, with the collector resistor R_C taking the place of the inverting amplifier feedback resistor and the emitter resistor R_E taking the place of the input resistor, so that the gain is

$$G = -\frac{R_C}{R_E}. \tag{7.1}$$

Unlike the op-amp inverting amplifier, the input impedance of the inverting amplifier is high relative to R_E, and is given by (6.8) as

$$Z_{IN} = (1+\beta)\cdot R_E. \tag{7.2}$$

Although the high resistances used by some op-amps may compensate for this impedance buffering effect, the BJT inverting amplifier is capable of very high performance with a very simple circuit. For AC coupled signal amplifiers, the BJT inverting amplifier is a good choice because of its simplicity relative to op-amp circuits, particularly if high gain-bandwidth product is required.

The process given in Section 6.3 provides a robust design using data sheet numbers, and can be completed without models such as SPICE, and provides uniform performance for normal variation in transistor performance parameters such as current gain β.

8 References

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